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Circuits and Architectures for the Implementation of Broadband Channelizers

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Circuits and Architectures for the Implementation of Broadband Channelizers

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In memory of

my beloved mother and father

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Circuits and Architectures for the Implementation of Broadband Channelizers

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Broadband spectrum channelizers sub-divide a broadband input spectrum into multiple sub-bands, where each of the sub-bands is down-converted and further processed at baseband. These designs can help to relax baseband design specifications. For example, baseband analog-to-digital converters (ADCs) that process the sub-bands at the channelizer output see only a part of the incident spectrum. The sampling frequency, and potentially the dynamic range of each sub-band ADC can thus be relaxed, compared to the case where a single ADC is used to digitize the full spectrum.

Spectrum channelizers can be used for multiple applications. These designs can be used as general-purpose hybrid frequency-and-time domain ADCs. The designs can also be employed for spectrum analysis, as well as for wireless communication applications.

In this dissertation, two circuit techniques for the implementation of broadband channelizers are proposed. A frequency-translational feedback-based interference canceler for attenuating large interferers at the output of the front-end low-noise amplifier (LNA) of a channelizer is shown. The design uses harmonic rejection mixers (HRMs) with embedded frequency synthesis capability. While channelizers reduce the bandwidth and potentially the dynamic range of the baseband ADCs, the analog signal paths in the channelizer can be broadband. Consequently the dynamic range required of the analog section of a sub-band path can still be limited by the presence of large signals in other, potentially distant parts of the spectrum. The demonstrated design is useful for relaxing the dynamic range requirement of the analog section that follows the front-end LNA in a channelizer. Reduction of the harmonic response and the frequency synthesizer tuning-range is also achieved in this design.

Second, a two-stage HRM is proposed which shares the same bias current between the RF and baseband stages, thus reducing the power consumption. Issues arising from bias-current sharing, such as the 1/f noise of the RF stage and potential degradation of the 2^{nd} harmonic response are identified, and circuit techniques are introduced to mitigate these potential degradation mechanisms.

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Chapter 1

Introduction

1.1 Overview

With the increasing number of wireless communication standards, modern radios need to have the ability to operate at several frequency bands. One way to implement such a radio is to employ multiple RF front-ends and baseband processors, each designed for a specific frequency band. However, it is challenging to integrate such an architecture on a single integrated circuit. A more efficient approach is to use a reconfigurable radio front-end that can be programmed to receive any frequency band. Such a radio is termed a software-defined radio [1][2][3].

Broadband channelizers, e.g., [4][5][6][7] offer a promising architecture for implementing software-defined radios. A typical channelizer may consist of a front-end with a parallel bank of mixers, each with a unique local oscillator. The input spectrum is down-converted by the mixers and then low-pass filtered, which decomposes the input into sub-bands. These sub-bands consist of signal information localized around the mixer LOs. The sub-band outputs are then digitized by baseband analog-to-digital converters (ADCs). Since the baseband ADCs see only a part of the input spectrum, the sampling frequency

and dynamic range requirement of these ADCs can be greatly relaxed.

In this research, circuit and architectural techniques for the design and implementation of broadband channelizers are investigated. Two key aspects are considered. The first relates to the linearity of the channelizer. In a broadband channelizer, a large signal in any sub-band of the input spectrum can appear as an interferer for a weak signal in any other sub-band. Such a large signal needs to be attenuated in order to relax the linearity requirement. Rejection of such an interferer at the input stage can be accomplished with a high-Q band-reject filter. However, such a filter is difficult to implement, primarily because it needs to be tunable in this application. A feedback-based interference cancellation technique that employs frequency-translated filtering is proposed for this purpose. The sub-band with the interferers is down-converted to baseband, low-pass filtered, up-converted and then subtracted from the input. Analog-frequency-synthesis capable harmonic-rejection-mixers (AFS-HRMs) are used in the down-conversion and up-conversion paths to suppress the harmonic response and reduce the required synthesizer tuning range.

The second design aspect is related to the down-conversion mixers employed in the channelizer. The power consumption of each harmonic rejection mixer (HRM) is critical as the number of channels becomes large. A bias-sharing scheme is implemented that re-uses the current between RF stage and baseband stage of the HRM to save power. Also, a two-stage HRM is used to make the harmonic rejection ratio (HRR) robust to process variation. Issues associated with the bias sharing scheme, such as degradation in 2^{nd} harmonic

rejection and impact of flicker noise are identified, and solutions are demonstrated.

1.2 Broadband Receiver Architectures

1.2.1 Direct RF Sampling Architecture

An ideal implementation of a programmable software-defined radio is shown in Fig. 1.1. A broadband low noise amplifier (LNA) amplifies the input signal and the following ADC samples and digitizes the input signal. Since the RF signal is directly sampled by the ADC, without any preceding frequency down-conversion, such an approach is termed direct RF sampling. The baseband digital signal processor (DSP) is then programmed to select the desired frequency band by digital filtering, and the information is demodulated and decoded.

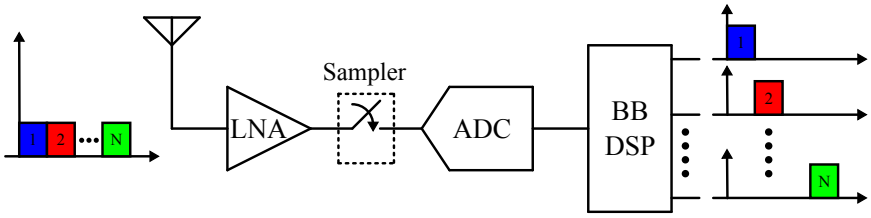


Figure 1.1: A software-defined radio

The most challenging building block in a direct RF sampling architecture is the ADC. Given that different communication standards have their own sensitivity and blocker specifications, the sampling speed and dynamic range requirement for the ADC can be stringent. A single-channel ADC can

potentially have high dynamic range, but its sampling speed may be limited for a given resolution, e.g., due to the time required to perform the conversion, as observed in successive approximation ADCs. A time-interleaved ADC architecture, on the other hand, can provide high operating frequency, but its dynamic range is limited due to the presence of various non-idealities such as mismatches between different channels and timing skew. Typically, if both high sampling speed and dynamic range requirements are to be satisfied, the power consumption of the ADC can be prohibitively high and unsuitable for mobile devices.

1.2.2 Channelized Front-End Architecture

An alternative approach for implementation of broadband radios is based on a channelized front-end. A broadband channelizer sub-divides a broadband input RF spectrum into M sub-bands, e.g., [7]. Each of the sub-bands is derived by down-conversion and filtering at baseband. The sub-bands may be further processed at baseband, after selection in the low-pass filter. A broadband channelized down-converter is shown in Fig. 1.2 for M=8. In this architecture, the front-end consists of a parallel bank of mixers, each with a unique local oscillator (LO). Since each of the baseband ADCs at the output of the low-pass filter (LPF) only sees part of the input spectrum, its sampling frequency and dynamic range requirement can be greatly relaxed.

A key challenge in the implementation of such designs is the linearity requirement of the channelizer front-end. A large sub-band will appear as the

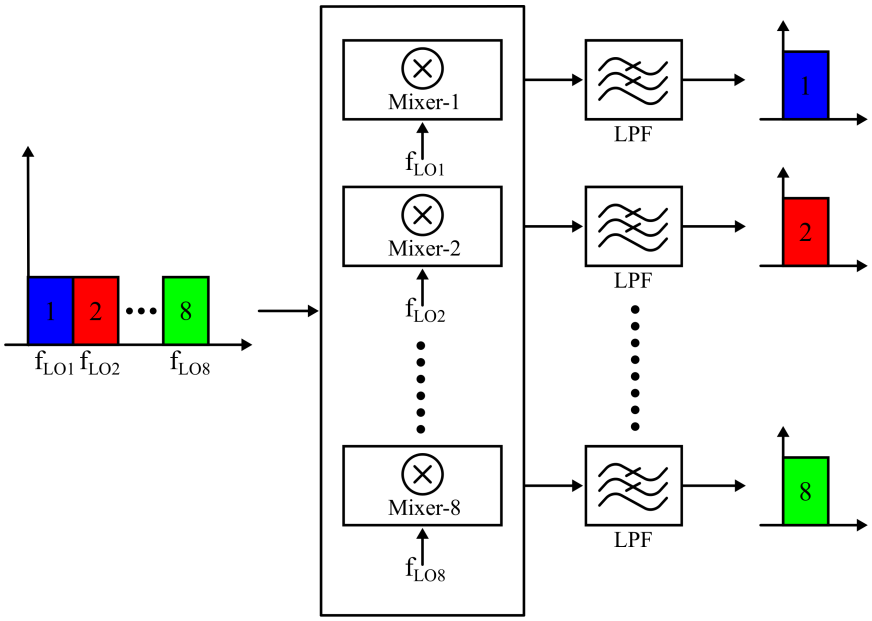


Figure 1.2: A broadband channelizer

interference to other sub-bands, and such interference needs to be attenuated as early as possible in the receiver chain, before further amplification. This is illustrated in Fig. 1.3. The large sub-band 2 (shown in red) needs to be suppressed in other paths in order not to be amplified by any following amplification.

A feedback-based interference cancellation technique is proposed to suppress sub-bands with large interferers. AFS-HRMs are used in both down-conversion and up-conversion paths to suppress the harmonic response and reduce the required synthesizer tuning range.

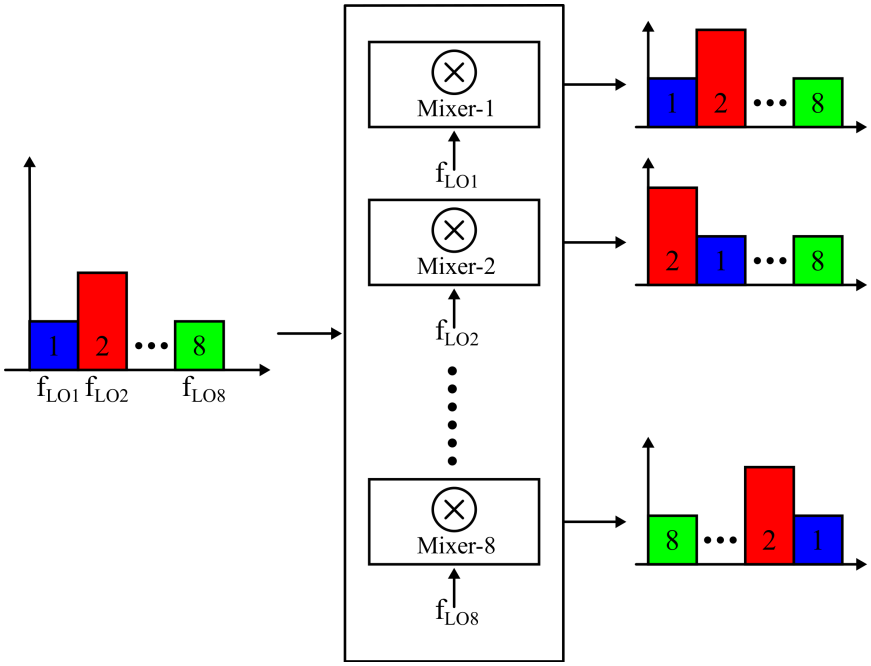


Figure 1.3: A large sub-band as interference for other sub-bands

A second challenge arises from the harmonic response of the mixers. Typically, mixers hard-limit the LO waveform to reduce the LO amplitude noise. The effective LO switching function contains not only the desired frequency, but also its harmonics. These undesired harmonics down-convert portions of the input spectrum, including interferers, around the harmonic frequencies to baseband, thereby degrading the signal-to-noise ratio (SNR) in the band of interest. This is illustrated in Fig. 1.4a.

Harmonic rejection mixers (HRMs) [8][9][10][11] are commonly used to down-convert only the desired portion of the input spectrum (Fig. 1.4b), while suppressing the harmonic response of the downconverter. A key design concern

in this case arises from the power consumption of these mixers, especially when the number of frequency-translation paths, M, becomes large, e.g., M=8. This is especially a challenge in mobile devices. Power reduction techniques for implementing HRMs are thus investigated.

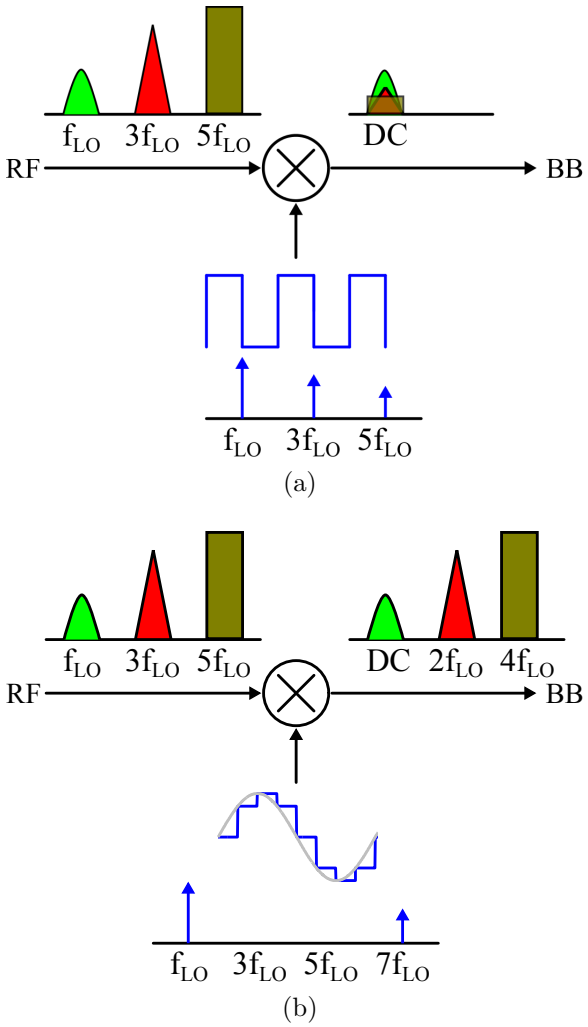


Figure 1.4: (a) Degradation of output SNR due to mixer harmonic response when interferer appears around harmonic frequencies (b) Mitigation of the effects of interferers around $2f_{LO}$ to $(N-2)f_{LO}$ by HRM

1.3 Review of Prior Art

1.3.1 Interference Cancellation Techniques

Active interference cancellation is a useful approach for suppressing large interferers within the front-end of the receiver chain in order to relax the linearity requirement of subsequent stages. Using such approaches, interferers can be rejected without the need of high-order tuned LC filters or external filters at RF. Feedforward and feedback are two main approaches implementing this technique, and will be discussed in the following.

Feedforward-based interference cancellation is proposed in [12], [13], [14]. The block diagram is shown in Fig. 1.5. The approach employs an auxiliary path in parallel with the main receiver path. The down-conversion mixer in the auxiliary path translates the desired signal to baseband. A nearby blocker is down-converted to a relatively higher frequency at the same time. A high-pass filter rejects the desired signal while allowing the blocker to pass through. An up-conversion mixer then up-converts the blocker to its original frequency, where it is subtracted from the main path.

The feedforward canceler partitions the dynamic range of the input between the main path and the auxiliary path. By reducing the interferer level in the main path, the linearity requirement of this path can be significantly reduced. Feedforward cancellation technique has the benefit of inherently stability. On the other hand, it needs careful matching of gain and phase of the main and auxiliary paths, over the bandwidth of interest.

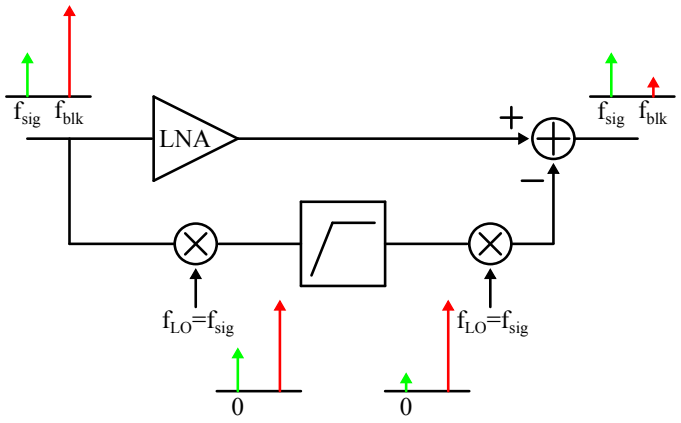


Figure 1.5: Feedforward-based interference cancellation

Feedback-based interference cancellation technique is proposed in [15]. The block diagram is shown in Fig. 1.6. In this approach, the down-conversion mixer translates a nearby blocker to baseband. A low-pass filter rejects the desired signal while only allowing the blocker to pass through. An up-conversion mixer then up-converts the blocker to its original frequency and subtracts it from the input in a feedback path. A similar technique has also been demonstrated in [16] where a high pass filter is used in baseband to reject the signal while allowing the blocker to be fed back. Feedback can reduce sensitivity to gain and phase mismatch between the main and auxiliary paths. However, its stability is not guaranteed and careful design is usually required.

In recent years, passive mixer based interference cancellation techniques have been proposed in [17][18][19][20]. This approach employs the ability of a passive mixer to transfer low-frequency impedance at its output to its RF input. A baseband low-pass response can be converted to an RF bandpass

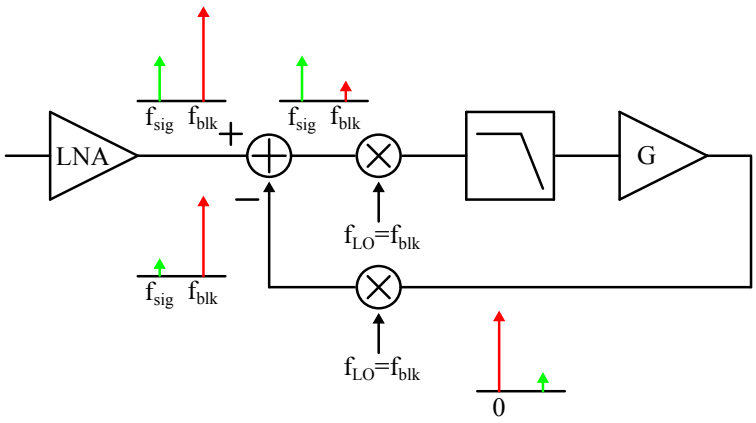


Figure 1.6: Feedback-based interference cancellation

response using this approach. Since the bandwidth of the low-pass response may be significantly smaller than the RF, the resulting bandpass filter can provide a very high effective quality factor. In [19], a passive I-Q mixer with 25% duty cycle LO frequency translates the baseband low-pass impedance to a RF band-pass response centered at the LO frequency. This is illustrated in Fig. 1.7. A notch filter response is described in [21] wherein the notch frequency can be tuned by changing the clock frequency.

Ideally, pure sinusoidal LOs should be employed in these filters [22], due to a lack of harmonic response. In practice, however, a pure sinusoidal LO is sensitive to amplitude noise and a discrete approximation of a sine wave, such as that achieved in HRMs, tends to be more robust.

1.3.2 Harmonic Rejection Mixers

As noted above, ideal rejection of all local oscillator (LO) harmonics requires the use of a multiplier with a sinusoidal LO. Practical mixers, however,

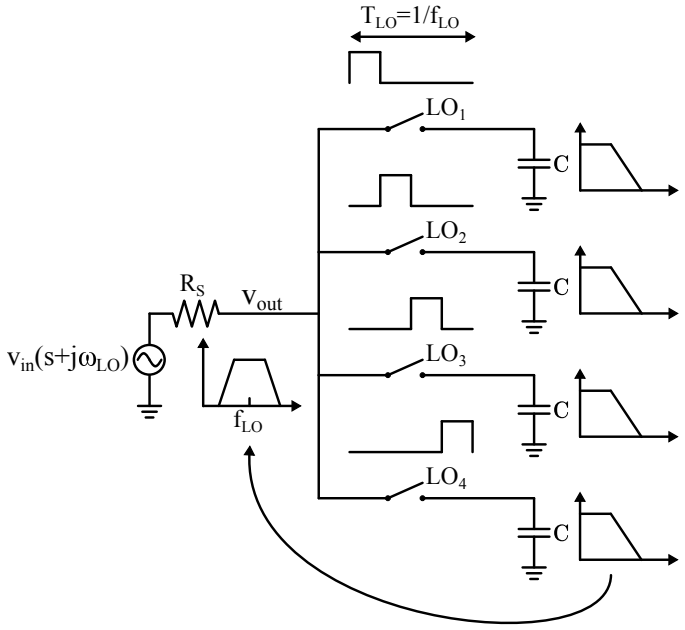


Figure 1.7: Impedance transfer in a passive mixer

amplitude-limit the LO signal, in order to make the gain independent of the LO amplitude and reduce SNR degradation due to LO amplitude noise. For instance, a current-commutating mixer internally converts a sinusoidal LO to a waveform that approximates a square-wave LO with 50% duty cycle. In this case, the n^{th} odd harmonic has a relative amplitude of $1/n$ compared to the fundamental, and can lead to significant spurious down-conversion.

Harmonic-rejection mixers (HRMs) first proposed in [8] can be used to down-convert broadband signals while mitigating folding of unwanted signals from harmonics of the down-conversion LO. Fig. 1.8 shows the equivalent down-conversion LO of an HRM and its corresponding spectrum. It can be seen that an HRM employs a synthesized LO with multiple discrete amplitude

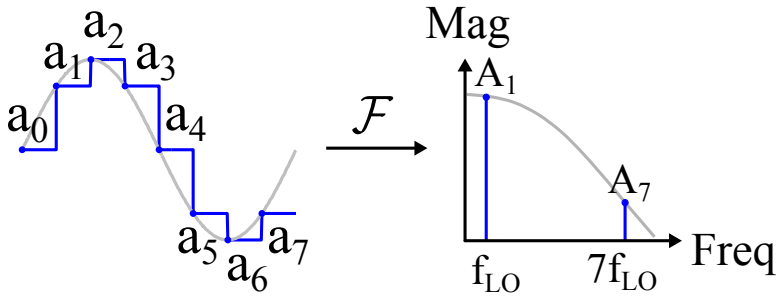


Figure 1.8: Synthesized LO waveform in an HRM and its spectrum

levels, which are equal to the values of a sinusoid sampled at discrete equispaced time steps, within one period. The synthesized LO thus approximates an ideal sinusoid. If a sinusoid with frequency f_{LO} is synthesized by a master LO with frequency Nf_{LO} (N=8 in Fig. 1.8), the spectrum of the synthesized LO will have harmonics at frequencies $(mN \pm 1)f_{LO}$ whose magnitude response (double-sided) is given by

$$A_{mN\pm1} = sinc\left(m \pm \frac{1}{N}\right) = \frac{sin\left(\pi\left(m \pm \frac{1}{N}\right)\right)}{\pi\left(m \pm \frac{1}{N}\right)}.$$

Since the first harmonic now appears at $(N-1)f_{LO}$, interferers around frequencies of $2f_{LO}$,....,$(N-2)f_{LO}$ will not be down-converted to baseband.

Fig. 1.9 shows an implementation of an HRM which synthesizes f_{LO} by using coefficients $a_k \propto sin(2\pi(k-1)/N)$, $k \in [1:N]$, along with non-overlapping clocks with duty-cycle of $1/N$, where N is set to 8 [23]. With ideal coefficients, a_k, complete rejection of specific harmonics can be observed, e.g., at $3f_{LO}$ and $5f_{LO}$. This requires the non-zero coefficients of a_k to be scaled with relative magnitudes of $1 : \sqrt{2} : 1$. In a practical implementation, ratios

involving irrational numbers are approximated by integer ratios, which can be implemented easily using device scaling. Thus a ratio such as $1 : \sqrt{2} : 1$ can be approximated by $5 : 7 : 5$. Random variations will also contribute to the non-ideal values of the gain coefficients a_k. Furthermore, the duty cycle of the non-overlapping clocks may not be exactly equal to $1/N$ due to process variations. These errors introduce unwanted spectral content around the ideally rejected harmonics, e.g., at $3f_{LO}$ and $5f_{LO}$, and degrade the harmonic rejection ratio (Fig. 1.9).

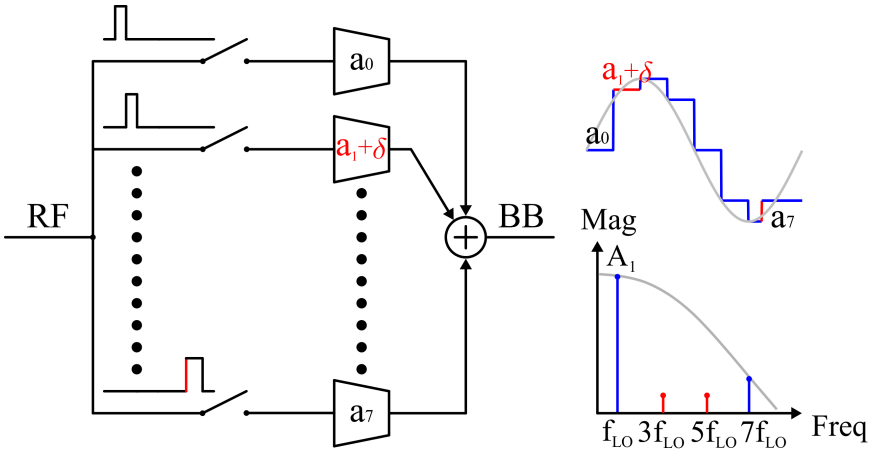


Figure 1.9: Spurious harmonic response around $3f_{LO}$ and $5f_{LO}$ in an HRM due to gain and phase errors

A two-stage harmonic rejection mixer architecture was proposed in [9] to mitigate the effect of amplitude non-idealities on HRR. In this approach, 2 sets of gain ratios, both of which approximate the ideal $1 : \sqrt{2} : 1$ ratio, are applied before and after the mixing. Clocks with duty cycle of $1/8$ ensure that the phase shift between the 8 paths is maintained at 45^{o}, hence the

second stage gain can further reject the harmonics around $3f_{LO}$ and $5f_{LO}$. Equivalently, these unwanted harmonics are rejected twice, and the resulting gain non-ideality becomes the product of the percentage mismatch in each stage, which makes this architecture more robust to gain non-idealities.

In order to mitigate the effect of clock phase errors on HRR, a clock re-timing technique was proposed in [10]. In this approach, a master clock with frequency Nf_{LO} was used in series with a non-overlapping phase-select clock. The phase-select clocks ideally have duty cycle 1/N and fundamental frequency f_{LO}, and can be generated from the master clock. In a practical implementation, the duty cycle of the phase-select clocks may vary due to process variation. The key observation here is that the mixing operation is dictated by the master clock, hence the errors in phase-select clocks have no impact on the HRR. Furthermore, since there is only one switch that is clocked by the master clock, no mismatch issue exists, either.

A two-stage harmonic rejection mixer with clock re-timing technique was proposed in [11]. By combining these two techniques, the HRR can be made robust to both amplitude and clock phase errors. Based on a principle similar to direct digital frequency synthesis (DDFS), an embedded frequency synthesis capability is also shown in [11]. A major advantage of such architecture is that the tuning range of the external master clock that is required to span a given frequency range for down-conversion is reduced.

1.4 Organization

This dissertation is organized as follows. In Chapter 2, a feedback-based interference cancellation technique using AFS-HRMs in both the down-conversion and up-conversion paths which reduces the unwanted harmonic response is proposed. By embedding frequency synthesis capability in the HRM similar to [11], the required synthesizer tuning range is also reduced. In Chapter 3, the harmonic transfer matrix technique is reviewed and is applied to the analysis of a 4-path frequency-translated band-pass filter. The maximum achievable rejection in the feedback based interference canceler proposed in Chapter 2 is derived. Chapter 4 proposes a bias-shared low-power two-stage HRM. Mechanisms relating to bias-sharing that can potentially degrade performance including flicker noise and even-order harmonic response are identified. Circuit techniques for mitigating these issues that exploit orthogonal phasing of RF and baseband signals are described. Conclusions and scope for future work are discussed in Chapter 5.

Chapter 2

An Active Interference Canceler with Reduced Harmonic Response and Synthesizer Tuning Range[1]

2.1 Introduction

This chapter describes a tunable interference canceler that employs a baseband low-pass filter within a frequency-translational feedback loop to suppress a high-frequency interferer. The interferer is down-converted to baseband, low-pass filtered, up-converted and then subtracted from the input. By using HRMs that are robust to gain and clock-timing mismatches in both down-conversion and up-conversion paths, the harmonic response of the canceler is reduced significantly in comparison to switch-based N-path filters. Furthermore, through the use of frequency-synthesis within the HRMs, the span of frequency synthesizer required to implement rejection over a given bandwidth is also significantly reduced.

The chapter is organized as follows: Sec. 2.2 provides a brief review of HRMs with frequency-synthesis capability (termed AFS-HRMs below) that

[1]Part of the material described in this chapter is based on [27], which was published in the IEEE Radio Frequency Integrated Circuits Symposium, 2015. The author Wei-Gi Ho was responsible for the design, and measurement of the IC described in the publication, and for theoretical analysis of the design.

are used in the feedback loop. Sec. 2.3 discusses the proposed interference canceler and Sec. 2.4 describes its circuit-level implementation. Techniques for desensitizing gain and clock timing mismatches are explained. Measurement results are shown in Sec. 2.5.

2.2 Principle of Analog Frequency Synthesis Capable Harmonic Rejection Mixers (AFS-HRM)

2.2.1 Spectrum of Sampled Sinusoid

Consider a sinusoid with frequency kf_{LO} sampled at frequency Nf_{LO}, where $k < N/2$. Assume that the sinusoid is denoted as $s(t) = cos(2\pi kf_{LO}t)$ and the resulting sampled version is denoted as $s_p(t)$, it follows that

$$s_p(t) = p(t) \times s(t) \tag{2.1}$$

where $p(t)$ is a train of impulses separated by $1/Nf_{LO} = T_{LO}/N$

$$p(t) = \sum_{n=-\infty}^{\infty} \delta(t + n\frac{T_{LO}}{N}). \tag{2.2}$$

Since multiplication in time domain corresponds to convolution in the frequency domain, the spectrum of $s_p(t)$ can be written as

$$S_p(f) = P(f) \otimes S(f) \tag{2.3}$$

where $P(f)$ and $S(f)$ are the Fourier transforms of $p(t)$ and $s(t)$, respectively

$$P(f) = \frac{N}{T_{LO}} \sum_{n=-\infty}^{\infty} \delta(f + n\frac{N}{T_{LO}}) \tag{2.4}$$

$$S(f) = \frac{1}{2}\delta(f - kf_{LO}) + \frac{1}{2}\delta(f + kf_{LO}). \tag{2.5}$$

Substituting Eq (2.4) and Eq (2.5) into Eq (2.3), we have

$$S_p(f) = \frac{N}{2T_{LO}} \sum_{n=-\infty}^{\infty} \delta(f - kf_{LO} + n\frac{N}{T_{LO}}) + \frac{N}{2T_{LO}} \sum_{n=-\infty}^{\infty} \delta(f + kf_{LO} + n\frac{N}{T_{LO}}). \tag{2.6}$$

From Eq (2.6), it can be observed that after sampling with impulse trains of period $1/Nf_{LO}$, a sinusoid with frequency kf_{LO} will have frequency components at $\pm kf_{LO} \pm nNf_{LO}$ for $n \in \mathbb{Z}$. This is illustrated in Fig. 2.1. As will be shown next, these are the only frequency components that will be present in the synthesized sinusoid that is used in the AFS-HRM.

2.2.2 Spectrum of a Synthesized Sinusoid

The sample-and-hold operation, illustrated in Fig. 2.2, can be modeled by first sampling with impulse functions followed by a filter with a rectangular impulse response [24]. The sampling function multiplies the input signal by an impulse train in the time domain. The corresponding spectrum is shown at the top of Fig. 2.2. The hold operation then holds the signal at the sampled value until the next sample is taken. This hold operation can be modeled as a convolution with an LTI filter with a rectangular impulse response given by

$$\begin{aligned} h(t) &= 1, \ for\ 0 < t < \frac{1}{Nf_{LO}} \\ &= 0, \ otherwise. \end{aligned}$$

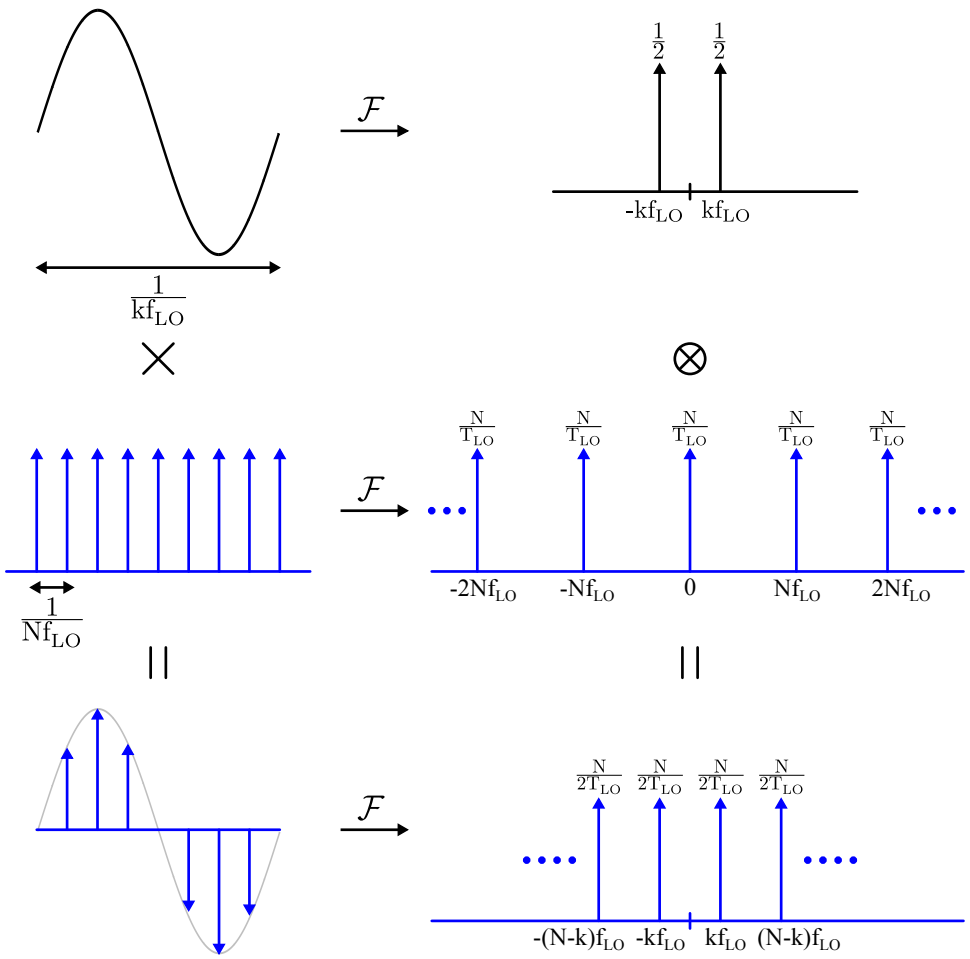


Figure 2.1: Sampling a sinusoid of frequency kf_{LO} by impulse trains with period $1/Nf_{LO}$ and the corresponding spectrum

The frequency response of this filter is a *sinc* function, given by

$$\begin{aligned} H(f) &= \frac{sin\left(\pi \frac{1}{Nf_{LO}} f\right)}{\pi f} e^{-j\pi \frac{f}{Nf_{LO}}} \\ &= \frac{1}{Nf_{LO}} sinc\left(\frac{f}{Nf_{LO}}\right) e^{-j\pi \frac{f}{Nf_{LO}}}. \end{aligned}$$

This is illustrated in the middle of Fig. 2.2. The convolution of the impulse-train sampled sinusoid with the rectangular pulse $h(t)$ in the time domain results in the sample-and-held sinusoid, which is denoted as $s_{sh}(t)$. Its spectrum, $S_{sh}(f)$, is the product of the corresponding spectrum of the impulse-train sampled sinusoid and the spectrum of $h(t)$

$$\begin{aligned} S_{sh}(f) &= \mathcal{F}\left[s_{sh}(t)\right] \\ &= \mathcal{F}\left[s_p(t) \otimes h(t)\right] \\ &= S_p(f) \times H(f) \\ &= \frac{1}{2} \sum_{n=-\infty}^{\infty} sinc\left(\frac{k}{N} - n\right) e^{-j\pi\left(\frac{k}{N} - n\right)} \delta(f - kf_{LO} + n\frac{N}{T_{LO}}) \\ &+ \frac{1}{2} \sum_{n=-\infty}^{\infty} sinc\left(\frac{k}{N} + n\right) e^{j\pi\left(\frac{k}{N} + n\right)} \delta(f + kf_{LO} + n\frac{N}{T_{LO}}). \end{aligned}$$

This is illustrated at the bottom of Fig. 2.2. The frequency components presented in the sampled sinusoid are further shaped by a *sinc* function.

2.2.3 AFS-HRM

The ability of an HRM to internally synthesize multiple harmonics was described in [25][11]. It is based on principles similar to direct digital frequency synthesis [26]. A discrete approximation of a sine wave with frequency kf_{LO}

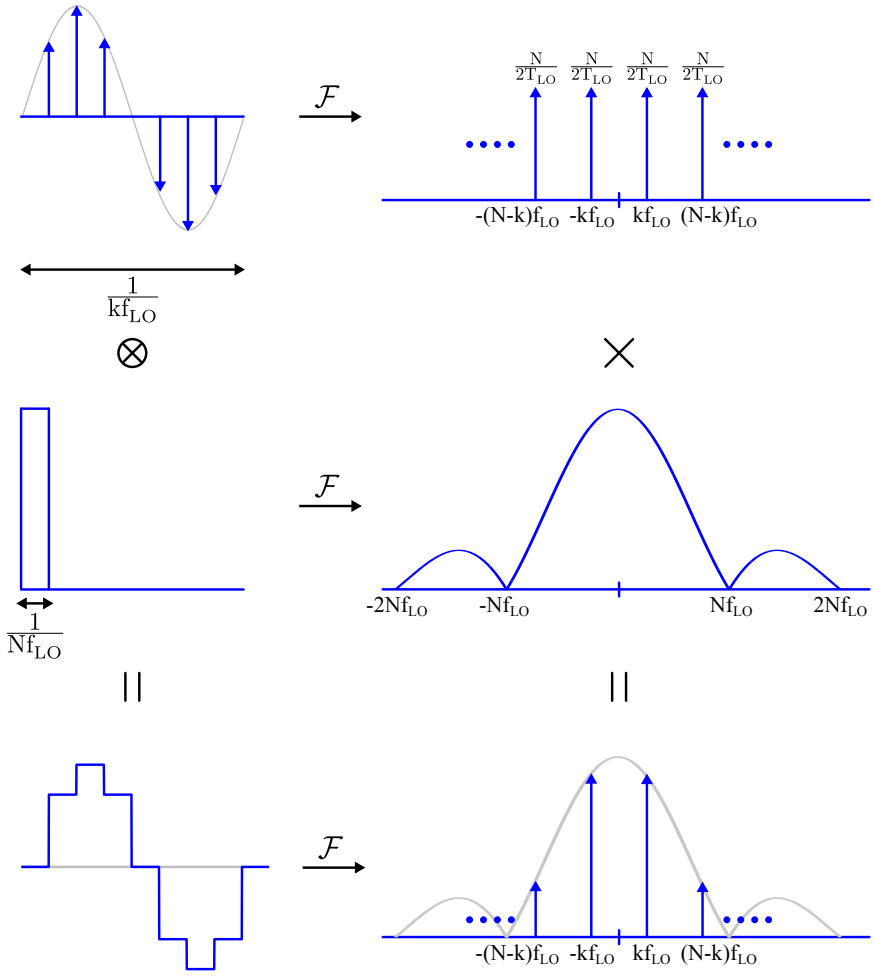


Figure 2.2: Sampling a sinusoid of frequency kf_{LO} by an impulse train with period $1/Nf_{LO}$, followed by holding the sampled value, in the time and frequency domains

can be synthesized by sampling a sine wave with master clock Nf_{LO}, followed by a zero-order hold. As discussed in Sec. 2.2.2, the synthesized sine wave will only contain frequency components of $(nN \pm k)f_{LO}$ for $n \in \mathbb{Z}$, where $\mathbb{Z}$ represents the set of integers. This is illustrated in Fig. 2.3 for $N = 8$ and $k = 1, 2, 3$. Fig. 2.3a shows phase clocks q_1-q_8 with fundamental frequency f_{LO} and duty cycle 1/8 as well as clocks q'_1-q'_4 with fundamental frequency $2f_{LO}$ and duty cycle 1/4. Both these phase clocks can be derived from a master clock (shown in the bottom of Fig. 2.3a) with fundamental frequency $8f_{LO}$ and duty cycle 1/2, which will be discussed in Sec. 2.4.1. Phase clocks q_1-q_8 are used to synthesize both f_{LO} and $3f_{LO}$, and phase clocks q'_1-q'_4 are used to synthesize $2f_{LO}$. These are illustrated in Fig. 2.3b, 2.3c and 2.3d, respectively. When an AFS-HRM is configured such that kf_{LO} is synthesized, we refer to it as operating in kf_{LO} mode.

As illustrated in Fig. 2.3, since the first undesired harmonic response of the synthesized frequency kf_{LO} is at $(N - k)f_{LO}$, in-band harmonic response is avoided as long as the band is limited to $\frac{N}{2}f_{LO}$. It is noted that the sample values a_p for $k = 3$ are just a reordering of those for $k = 1$ in time, while sample values a_p for $k = 2$ are a subset of those for $k = 1$. The sample values a_p can be written as

$$a_p = sin\left(\frac{2\pi k}{N}p\right), \tag{2.7}$$

and the spectral content $A_{\ell N \pm k}$ around $(\ell N \pm k)f_{LO}$ is

$$A_{\ell N \pm k} = sinc\left(\ell \pm \frac{k}{N}\right) = \frac{sin\left(\left(\ell \pm \frac{k}{N}\right)\pi\right)}{\left(\ell \pm \frac{k}{N}\right)\pi}. \tag{2.8}$$

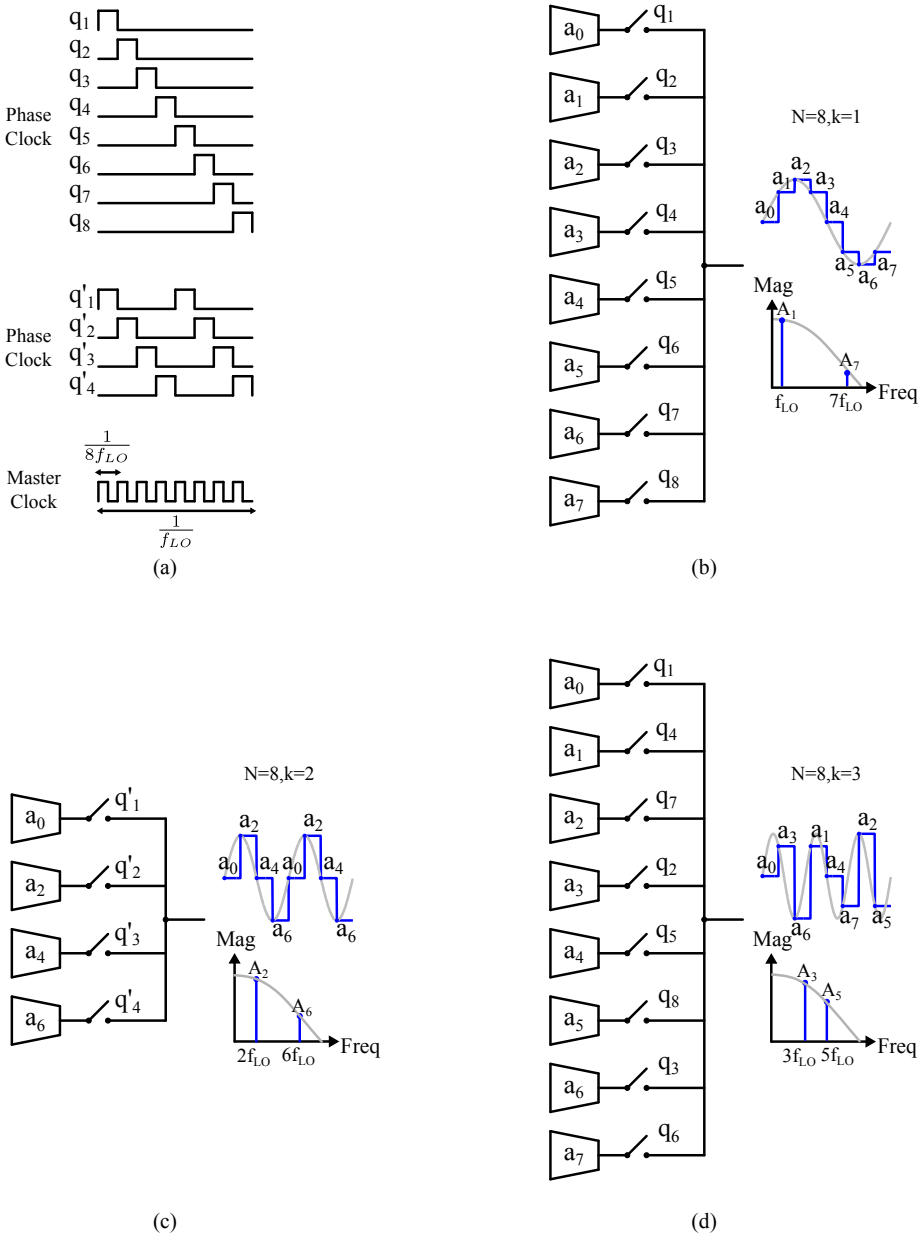


Figure 2.3: The operating principle of an AFS-HRM (a) The phase clocks and master clock (b) LO waveform and corresponding spectrum for f_{LO} mode (c) LO waveform and corresponding spectrum for $2f_{LO}$ mode (d) LO waveform and corresponding spectrum for $3f_{LO}$ mode

In Sec. 3.4.3, we will see that the magnitude of $A_{\ell N \pm k}$ for $\ell \neq 0$ will play a key role in the maximum achievable rejection of the proposed interference canceler.

2.3 Proposed Interference Canceler

The proposed interference canceler is shown in Fig. 2.4 [27]. The input signal is amplified by a broadband amplifier **A**. An 8-path frequency-translated negative feedback loop is used to cancel the interferer at the output of **A**. The interferer is down-converted to baseband within the loop, where it is selected by a baseband low-pass filter (BB-LPF). The selected interferer is then up-converted and subtracted from the output of the amplifier **A** in the current domain. Through use of the frequency-translation loop, only the portion of the input spectrum that is selected by the low-pass filter in the loop is rejected at V_{out}. The other part of the input spectrum can then be down-converted in a separate path, which will require significantly lower dynamic range, if large interference is already rejected at V_{out}.

As shown in Fig. 2.4, AFS-HRMs are employed to synthesize an equivalent down-conversion and up-conversion frequency, which is identical to the interferer frequency, based on an external master clock. If the input spectrum has a bandwidth of $4f_{LO}$, the first unwanted harmonic response of an 8-phase AFS-HRM will still be out-of-band ($(N-k)f_{LO} > 4f_{LO}$ for $N = 8,\ k = 1, 2, 3$), as discussed previously. The use of 8-paths helps to suppress harmonic foldings, which will be discussed in Chapter 3.

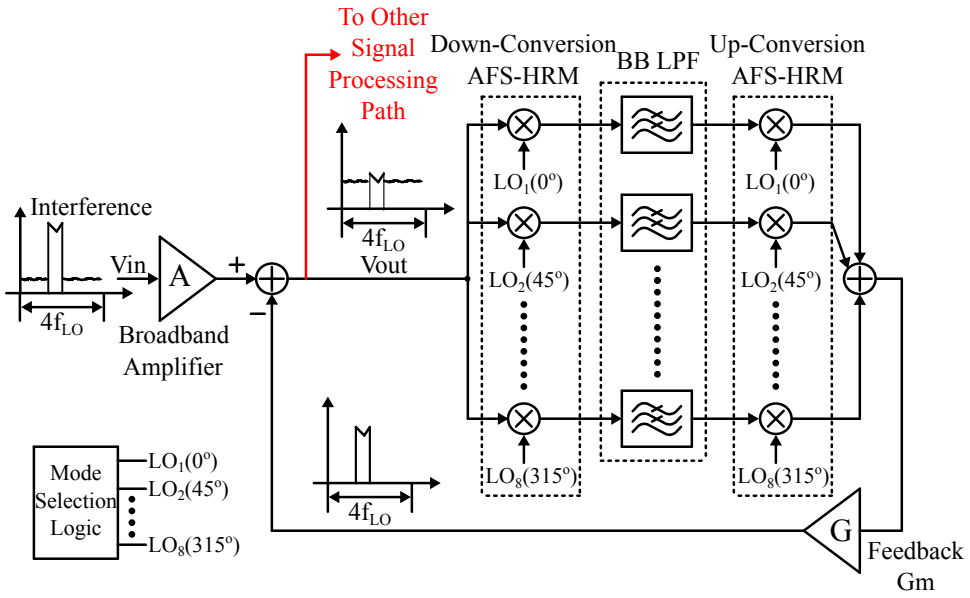


Figure 2.4: Block diagram of the proposed interference canceler

The equivalent down-conversion waveform for LO_1-LO_8 in Fig. 2.4 is shown in Fig. 2.5 for the f_{LO} mode. As can be seen, the phase difference amongst these waveforms is a multiple of 45°. For $2f_{LO}$ and $3f_{LO}$ mode, the waveforms will be phase-shifted versions of Fig. 2.3c and Fig. 2.3d, respectively. Sec. 2.4.1 will describe how to synthesize these down-conversion waveforms in a practical implementation.

In addition to reduced harmonic response, the use of an AFS-HRM also helps to reduce the tuning range that is required of the frequency synthesizer. Assume that $N = 8$ with an input bandwidth of $4f_{LO}$. For an interferer at any given frequency within this band, different operating modes of the AFS-HRM can be selected in order to reduce the synthesizer tuning range. When the interferer frequency is in the range of 0-1.5f_{LO}, f_{LO} mode (k=1) is

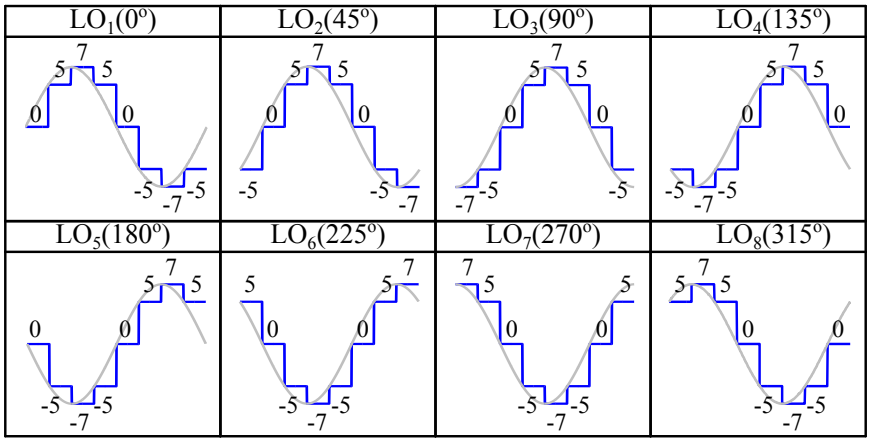


Figure 2.5: The equivalent down-conversion waveforms for $LO_1(0^o)$-$LO_8(315^o)$ in the f_{LO} mode

used and the required master clock tuning range is 0-$(1.5 \times 8)f_{LO}$=0-$12f_{LO}$. Similarly, when the interferer frequency is in the range of $1.5f_{LO}$-$2.5f_{LO}$ and $2.5f_{LO}$-$4f_{LO}$, $2f_{LO}$ mode and $3f_{LO}$ mode will be used and the corresponding required master clock tuning range will be $(1.5\times8/2)f_{LO}$-$(2.5\times8/2)f_{LO}$=$6f_{LO}$-$10f_{LO}$ and $(2.5 \times 8/3)f_{LO}$-$(4 \times 8/3)f_{LO}$=$6.7f_{LO}$-$10.7f_{LO}$, respectively. This is illustrated in Fig. 2.6. Hence if the AFS-HRM is used, the required master clock frequency span is $12f_{LO}$. Without an AFS-HRM, the required tuning master clock span can be as high as $4f_{LO} \times 8 = 32f_{LO}$, since traditional HRMs only operate in the f_{LO} mode. If 16-phase HRMs are utilized, similar to [11], 8 effective harmonics can be synthesized in the HRMs to further reduce the span of the external synthesizer, although at the expense of higher design complexity compared to the 8-phase designs employed here.

Interference Location	Operating Mode	Master Clock
0-1.5f_{LO}	f_{LO}	0-12f_{LO}
1.5-2.5f_{LO}	2f_{LO}	6-10f_{LO}
2.5-4f_{LO}	3f_{LO}	6.7-10.7f_{LO}

Figure 2.6: The interference location and the corresponding operating mode of the AFS-HRM

2.4 Circuit Implementation

2.4.1 Down-Conversion AFS-HRM

The down-conversion AFS-HRM is shown in Fig. 2.7a. Transconductors with ratios 0:5:7:5:0:-5:-7:-5 are used to approximate the ideal gain ratios 0:1:$\sqrt{2}$:1:0:-1:$-\sqrt{2}$:-1. The transconductor with zero-gain is shown in the figure for clarity and is not implemented in the actual circuit. Simple CMOS inverters, biased at the mid-supply, are chosen as the transconductor cells (Fig. 2.7b). Small source-degeneration resistors are used to increase the output impedance of the transconductors. The switch bank shown in Fig. 2.7c consists of eight clock-gated switches, whose operation is discussed below. It connects the output of the transconductor to different outputs (OUT_1-OUT_8) during different time slots.

The clock-gated switches used in the switch bank of the down-conversion AFS-HRM are shown in Fig. 2.8. It is similar to that used in [11], and is implemented using NMOS switches. As illustrated in Fig. 2.8a, it consists of two sets of switches. The gain-steering switches steer the input signal to the output at specific time intervals when the phase clocks ($q_i\pm$) are high, while

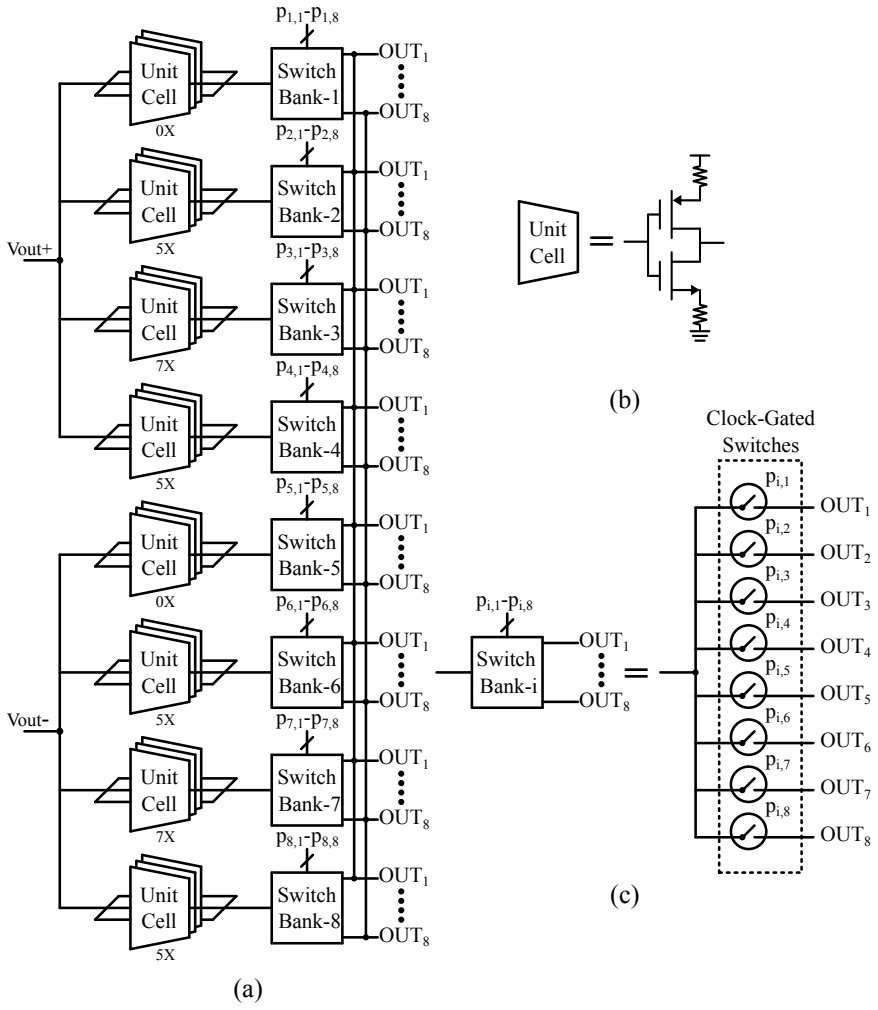


Figure 2.7: (a) Block diagram of the down-conversion AFS-HRM (b) Implementation of unit-cell (c) Switch bank consisting of eight re-timing switches

the re-timing switches clocked by the master clocks (CLK±) control the exact time at which the input is steered to the output [28][10]. Similar techniques have also been demonstrated for enhancing image rejection [29] and for reducing the impact of flicker noise [30]. The relative timing between the phase clocks and the master clocks is shown in Fig. 2.8b. It can be seen that the variations of the rising and falling edges of the phase clocks have no effect on the equivalent controlling pulse q_{eq} as long as the phase clocks $q_i\pm$ remain high when the master clocks CLK± are high. It follows that q_{eq} is determined only by the master clock and is insensitive to the edge variations of the phase clocks $q_i\pm$.

The phase clocks $q_i\pm$ (Fig. 2.8c) with fundamental frequency f_{LO} and duty cycle 1/8 are generated by connecting 8 flip-flops in a ring. The flip-flops are implemented using true-single-phase-clocking (TSPC) [31] logic and are clocked by the master clocks CLK± that have a fundamental frequency of $8f_{LO}$ and a duty-cycle of 50%. In the reset mode, only the first flip-flop stores one, while the other 7 flip-flops store a zero. When the operation is enabled, the one stored in the first flip-flop propagates through the flip-flop ring, generating the required phase clocks $q_i\pm$. These phase clocks are used when the down-conversion AFS-HRM is operated in the f_{LO} and $3f_{LO}$ modes. Phase clocks q_i' (Fig. 2.3a) that are used in the $2f_{LO}$ mode can be similarly generated by connecting 4 flip-flops in a ring.

Mode-selection logic maps the ring flip-flop outputs (q_i's in Fig. 2.8c) to proper $p_{x,y}$'s in Fig. 2.7a according to the selected operating mode. The

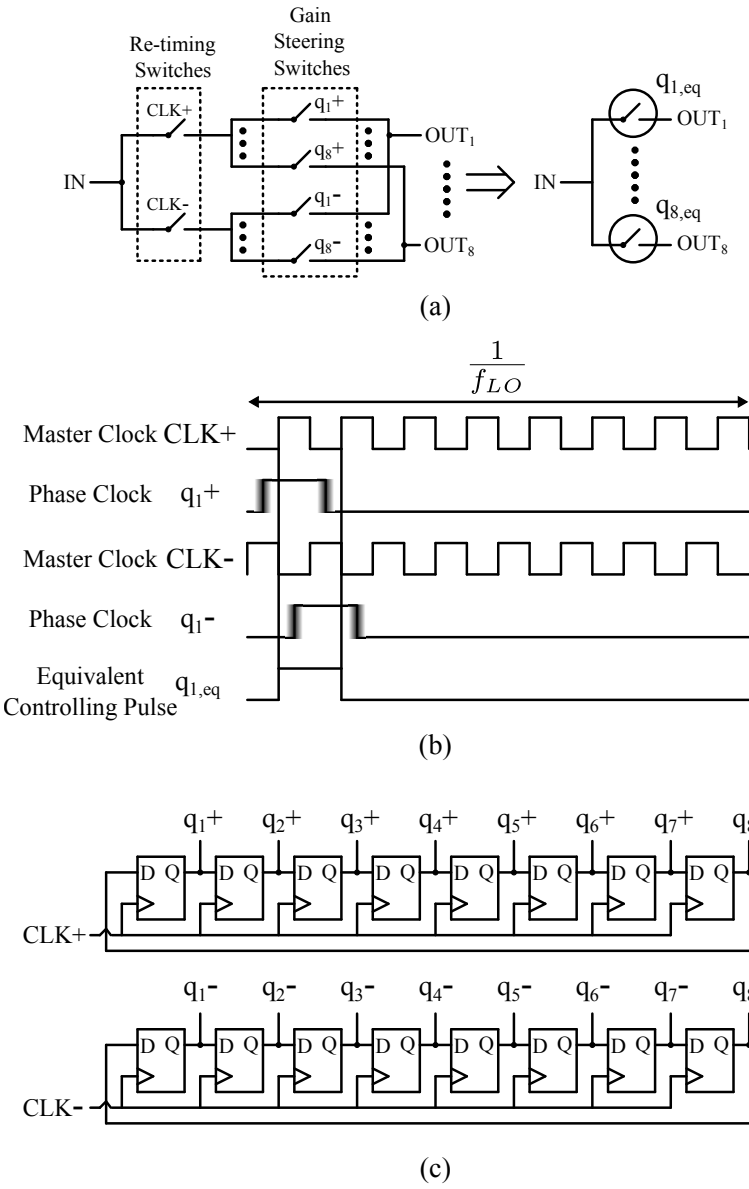
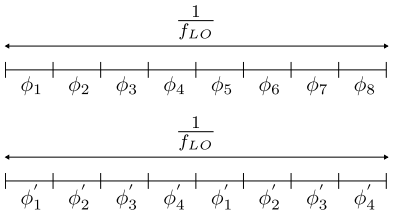


Figure 2.8: The switching used in the down-conversion AFS-HRM (a) The clock-gated switch consisting of re-timing switches and gain-steering switches (b) Relative timing between master clocks and phase clocks (c) Generation of phase clocks from master clocks by 8 flip-flops connected in a ring

selection logic determines the time slot ϕ_1-ϕ_8 (Fig. 2.9 top) when a transconductor cell is connected to a specific output, and hence the synthesized down-conversion frequency. This is summarized in Fig. 2.9a, 2.9b and 2.9c, respectively. The terms 5a and 5b are used to designate the two different cells with gain of 5 in Fig. 2.7a. Following the ϕ_1-ϕ_8 sequence, the synthesized down-conversion waveform at a specific output can be read from Fig. 2.9. For example, at OUT_1, [0 5a 7 5b 0 -5a -7 -5b] synthesizes the f_{LO} mode, while [0 7 0 -7 0 7 0 -7] and [0 5b -7 5a 0 -5b 7 -5a] synthesize the $2f_{LO}$ and $3f_{LO}$ modes, respectively. It can also be seen that timing sequence for the f_{LO} mode in Fig. 2.9a synthesizes exactly the same equivalent down-conversion waveforms as shown in Fig. 2.5.

The use of 8 paths and clock-gated switches in the switch bank ensures that the relative phase shift amongst the outputs OUT_1-OUT_8 is at multiples of 45°, even in the presence of variations in the transconductor gain or timing variations in the re-timing switches used in the switch bank. This is illustrated in Fig. 2.10 for the f_{LO} mode. The variations in the transconductor gain and re-timing switches are shown in red. Since the same variation appears across all outputs, the relative 45° phase relation is maintained. Such a phase relation has the benefit of reducing undesired harmonic foldings, which will be discussed in Sec. 3.4.3.2.



	OUT_1	OUT_2	OUT_3	OUT_4	OUT_5	OUT_6	OUT_7	OUT_8
0	ϕ_1	ϕ_2	ϕ_3	ϕ_4	ϕ_5	ϕ_6	ϕ_7	ϕ_8
5a	ϕ_2	ϕ_3	ϕ_4	ϕ_5	ϕ_6	ϕ_7	ϕ_8	ϕ_1
7	ϕ_3	ϕ_4	ϕ_5	ϕ_6	ϕ_7	ϕ_8	ϕ_1	ϕ_2
5b	ϕ_4	ϕ_5	ϕ_6	ϕ_7	ϕ_8	ϕ_1	ϕ_2	ϕ_3
0	ϕ_5	ϕ_6	ϕ_7	ϕ_8	ϕ_1	ϕ_2	ϕ_3	ϕ_4
-5a	ϕ_6	ϕ_7	ϕ_8	ϕ_1	ϕ_2	ϕ_3	ϕ_4	ϕ_5
-7	ϕ_7	ϕ_8	ϕ_1	ϕ_2	ϕ_3	ϕ_4	ϕ_5	ϕ_6
-5b	ϕ_8	ϕ_1	ϕ_2	ϕ_3	ϕ_4	ϕ_5	ϕ_6	ϕ_7

(a)

	OUT_1	OUT_2	OUT_3	OUT_4	OUT_5	OUT_6	OUT_7	OUT_8
0	ϕ_1'	×	ϕ_2'	×	ϕ_3'	×	ϕ_4'	×
5a	×	ϕ_2'	×	ϕ_3'	×	ϕ_4'	×	ϕ_1'
7	ϕ_2'	×	ϕ_3'	×	ϕ_4'	×	ϕ_1'	×
5b	×	ϕ_3'	×	ϕ_4'	×	ϕ_1'	×	ϕ_2'
0	ϕ_3'	×	ϕ_4'	×	ϕ_1'	×	ϕ_2'	×
-5a	×	ϕ_4'	×	ϕ_1'	×	ϕ_2'	×	ϕ_3'
-7	ϕ_4'	×	ϕ_1'	×	ϕ_2'	×	ϕ_3'	×
-5b	×	ϕ_1'	×	ϕ_2'	×	ϕ_3'	×	ϕ_4'

(b)

	OUT_1	OUT_2	OUT_3	OUT_4	OUT_5	OUT_6	OUT_7	OUT_8
0	ϕ_1	ϕ_4	ϕ_7	ϕ_2	ϕ_5	ϕ_8	ϕ_3	ϕ_6
5a	ϕ_4	ϕ_7	ϕ_2	ϕ_5	ϕ_8	ϕ_3	ϕ_6	ϕ_1
7	ϕ_7	ϕ_2	ϕ_5	ϕ_8	ϕ_3	ϕ_6	ϕ_1	ϕ_4
5b	ϕ_2	ϕ_5	ϕ_8	ϕ_3	ϕ_6	ϕ_1	ϕ_4	ϕ_7
0	ϕ_5	ϕ_8	ϕ_3	ϕ_6	ϕ_1	ϕ_4	ϕ_7	ϕ_2
-5a	ϕ_8	ϕ_3	ϕ_6	ϕ_1	ϕ_4	ϕ_7	ϕ_2	ϕ_5
-7	ϕ_3	ϕ_6	ϕ_1	ϕ_4	ϕ_7	ϕ_2	ϕ_5	ϕ_8
-5b	ϕ_6	ϕ_1	ϕ_4	ϕ_7	ϕ_2	ϕ_5	ϕ_8	ϕ_3

(c)

Figure 2.9: The timing sequence for the transconductors connected to various outputs for different operating modes (a) f_{LO} (b) $2f_{LO}$ (c) $3f_{LO}$

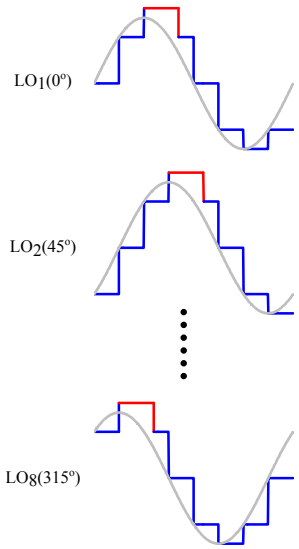


Figure 2.10: 45° phase shift among the paths in the presence of gain and timing variations (shown in red)

2.4.2 Baseband Filtering

The outputs of the passive switches (OUT_1-OUT_8 in Fig. 2.7) in the down-conversion AFS-HRMs are connected to low impedance common-gate amplifiers, that provide I-V conversion. This is illustrated in Fig. 2.11. The down-converted baseband current is then mirrored at the cascode output [11], where it is applied to a single-pole RC low-pass filter. First-order baseband low-pass filtering is thus used in the interference canceler to select the interferer while rejecting the signals which are located in other portions of the input spectrum. The selected interference will then be up-converted and subtracted from the input. Higher order low-pass filters can also be used in the baseband, which needs more design effort to ensure stability.

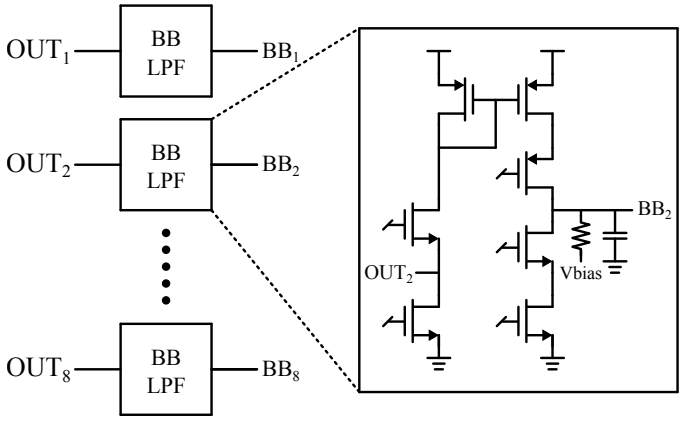


Figure 2.11: Baseband first-order low-pass filtering

2.4.3 Up-Conversion Path

The up-conversion path consists of up-conversion AFS-HRMs, combining trans-impedance amplifiers (TIAs) and feedback transconductance, as illustrated in Fig. 2.12. The up-conversion AFS-HRM is implemented in a similar way as the down-conversion AFS-HRM. The up-conversion AFS-HRM configured in the f_{LO} mode is shown in Fig. 2.12. In the first path with input BB_1, a ratio 0:5:7:5:0:-5:-7:-5 is synthesized as 5×[0 1 1 1 0 -1 -1 -1]+2×[0 0 1 0 0 0 -1 0]. Similarly, in the 8^{th} path with input BB_8, ratio 5:7:5:0:-5:-7:-5:0 is synthesized as 5×[1 1 1 0 -1 -1 -1 0]+2×[0 1 0 0 0 -1 0 0]. The equivalent synthesized up-conversion LO waveform is also shown in Fig. 2.12. A switch bank and selection logic similar to the down-conversion AFS-HRM is used to re-configure the up-conversion AFS-HRM to operate in different modes. The up-conversion transconductance cells are implemented as PMOS common-source amplifiers with resistor loads. This helps to mitigate the po-

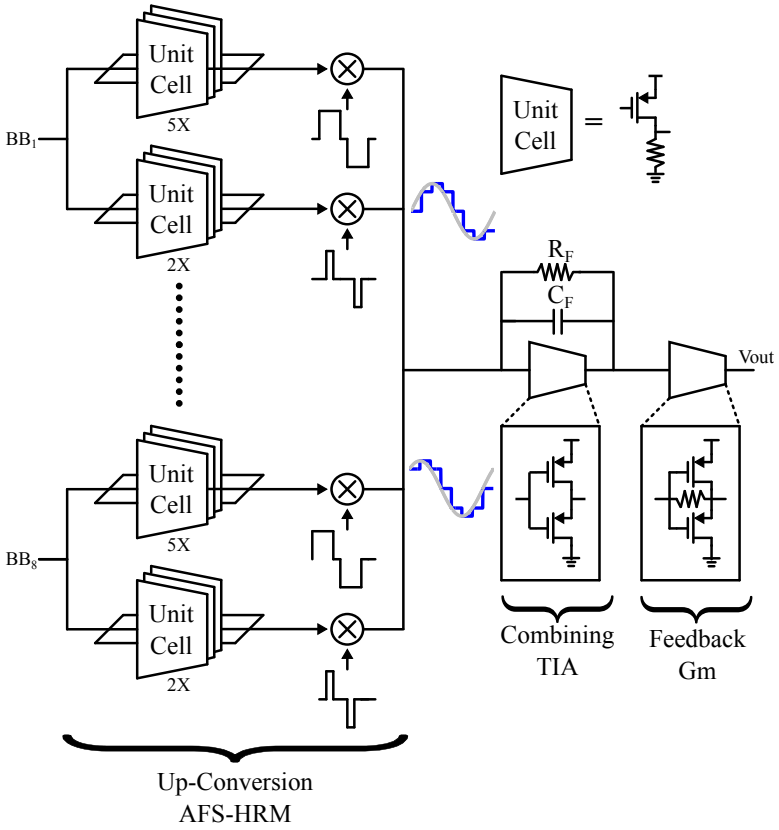


Figure 2.12: The up-conversion path consisting of an up-conversion AFS-HRM, a combining TIA and a feedback G_m

tential degradation due to up-converted flicker noise arising from non-ideal harmonic rejection since the flicker noise performance of PMOS is better than that of NMOS devices in the process that was employed.

The transconductance cell used in the up-conversion path TIA is implemented as a CMOS inverter. It converts the input current to voltage at its

output. The input impedance Z_{in} and the trans-impedance gain Z_G are

$$Z_{in} = \frac{\frac{R_F}{1+sR_FC_F} + r_o}{1 + g_m r_o} \tag{2.9}$$

$$Z_G = \frac{-1}{1 + g_m r_o} \left\{ \frac{g_m r_o R_F}{1 + sR_FC_F} - r_o \right\}, \tag{2.10}$$

where g_m is the transconductance of the CMOS inverter and r_o is its output resistance. It provides a low-impedance termination for the outputs of the up-conversion switches, lowering the swing at the switch output which helps linearity. The capacitor C_F, in parallel with the shunt feedback resistance R_F, is used to attenuate the harmonic response beyond the bandwidth $4f_{LO}$, which improves the achievable rejection (Eq (3.33) and Eq (3.34)). The feedback transconductance cell is implemented as a self-biased inverter. It converts the interferer into current, which is then subtracted at the node V_{out} in the current domain to suppress the interferer.

2.4.4 Feedback Path Optimization

In order to reject a large interferer, the feedback G_m (Fig. 2.12) must have sufficient current-handling capability. The loop will in fact reject the interferer up to the level where the feedback transconductor operates linearly. Thus the feedback G_m must have a value comparable to the transconductance of the broadband amplifier **A** in Fig. 2.4.

This introduces a noise vs. linearity trade-off in the feedback loop. If the feedback G_m is identical to that of **A**, the active noise sources observed by

signals away from the interferer will nearly double, thus degrading the noise figure. It is noted that the overall dynamic range can be improved significantly, since the improvement in compression point, and IIP3 can considerably exceed the degradation in noise figure.

It can be observed from Fig. 2.4, that outside the rejection-band, the BB-LPF effectively suppresses the noise of the down-converter. The noise injection into the signal path is thus determined primarily by the up-conversion path. As noted above, the feedback G_m is one noise contributor in this path. Another important contributor is the up-converted noise of the baseband PMOS unit-cells. When the design operates in the kf_{LO} modes, baseband noise at frequency f_{BB} is up-converted to $f_{BB} + k \cdot f_{LO}$ by the up-conversion mixer. The amount of this noise is proportional to the transconductance of the PMOS unit cells ($g_{mp,BB}$).

The small-signal rejection is determined by the loop-gain of the system $H_0(s)$ in Eq (3.33) and Eq (3.34). This term itself consists of the gain provided by the BB-LPF, $g_{mp,BB}$ and the feedback G_m. In a small-signal sense, it is possible to make $H_0(s)$ large by moving a majority of the gain to the BB-LPF and using small values for $g_{mp,BB}$ and feedback G_m. If the key design care-about is enhancing IIP3, which is a relatively small-signal consideration, this is a valid approach. However in order to boost blocker-induced compression, where a physically large signal is applied to the input, it is important to use a sufficiently large feedback G_m to provide adequate signal-handling capability, as described in the prior paragraph.

Another significant consideration in the design is the up-conversion of flicker noise of $g_{mp,BB}$ to harmonics other than kf_{LO}. In order to reduce the impact of this noise source on the noise figure observed by a signal at the harmonic bands, the spurious response of the up-conversion HRM needs to be minimized. While the inherent rejection of a first-order HRM is of the order of 30 dB, calibration of gain cells can be beneficially used here, if required. The impact of this flicker noise source is observed within the flicker noise corner of the baseband PMOS transconductors. Thus a second means to mitigate this noise source, and minimizing the bandwidth over which flicker noise is a consideration, is by using large devices in the baseband transconductance PMOS devices.

2.5 Measurements

The interference cancellation technique is implemented in a 65nm CMOS process. The master clocks are derived from an externally applied sinusoidal signal. An on-chip clock buffer is used to generate 50% duty-cycle square waves, which are then used as the clocks for the switch-bank (Fig. 2.8). The active chip area is approximately 1000×880 μm^2 (Fig. 2.13). The design was measured in a QFN package on a PCB. An external differential-to-single-ended unity gain buffer was employed to interface the IC to the spectrum analyzer.

The full bandwidth of the input signal was chosen to be 250 MHz. In-band harmonic folding is measured to be better than -40 dB (Fig. 2.14). This measures the gain from the input frequency at $f_{in}+kf_{LO}$ to another frequency

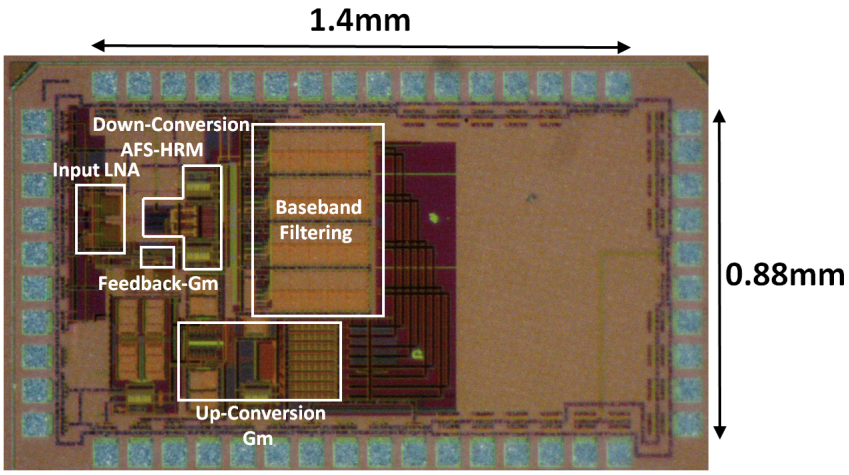


Figure 2.13: Die photograph

$f_{in} + mf_{LO}$ when the canceler is operating in kf_{LO} mode. The values of m are indicated on the X-axis of the figure.

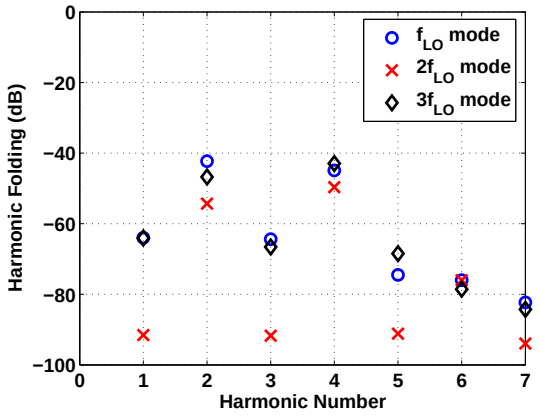


Figure 2.14: Measured harmonic folding

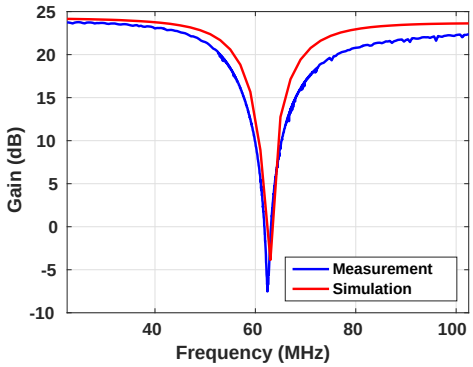
The measured frequency response is compared to the simulation result for master clock frequency of 500 MHz for various operating modes near the

notch response frequency, which is shown in Fig. 2.15. The notch response of the proposed technique with master clock frequency tuned from 400 MHz to 625 MHz in various modes is shown in Fig. 2.16. Due to the use of AFS-HRMs in both down-conversion and up-conversion paths, there is no harmonic null response across the input band. The achieved small-signal rejection for f_{LO} and $2f_{LO}$ modes is approximately 25 dB, and for the $3f_{LO}$ mode it is approximately 15 dB.

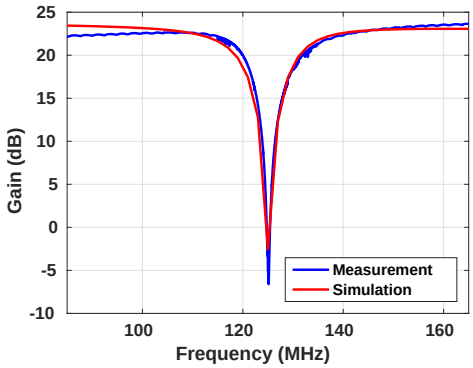
The total external LO span for rejecting a blocker anywhere between 0-250 MHz is 750 MHz. Without the use of AFS-HRMs, the required span would be 2 GHz.

Linearity is measured with and without the interference cancellation technique. The desired input signal is located 40 MHz away from the blocker and the notch response is tuned to the blocker frequency. An improvement of the blocker-induced 1-dB compression of 8-13 dB is observed (Fig. 2.17). The IIP3 also shows 17 dB (f_{LO} mode) to 6 dB ($3f_{LO}$ mode) improvement (Fig. 2.18). The noise figure without and with the interference cancellation is 4.5 dB and 7 dB, respectively.

The proposed technique consumes analog power of 33.8 mA, with nearly 60% used in the up-conversion G_M, and digital power of 7.6 mA. The supply voltage is 1.4 V for the baseband section and the up-conversion AFS-HRM, while 1.2 V for all other analog and digital parts. The performance is summarized and compared with other similar designs in Table-2.1.



(a)



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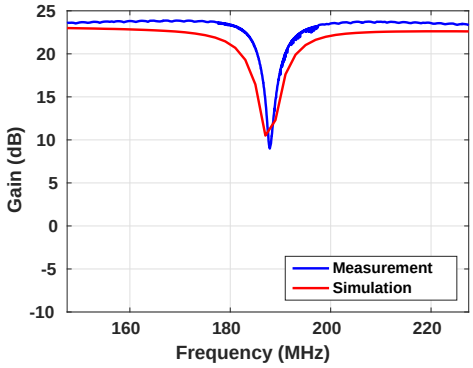
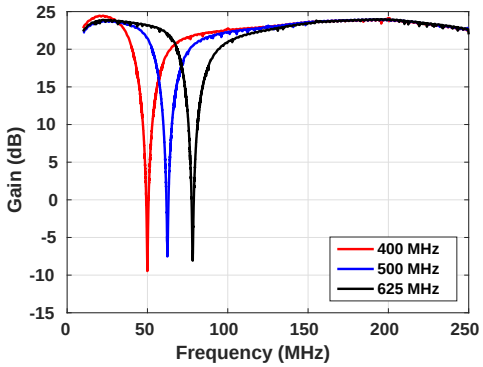
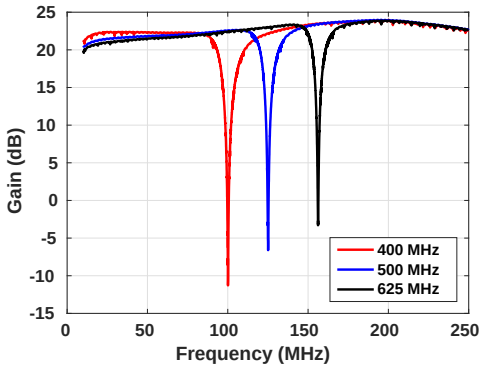


(c)

Figure 2.15: Measurement and simulation of gain response near the notch frequency for a master clock frequency of 500 MHz (a) f_{LO} mode (b) $2f_{LO}$ mode (c) $3f_{LO}$ mode



(a)



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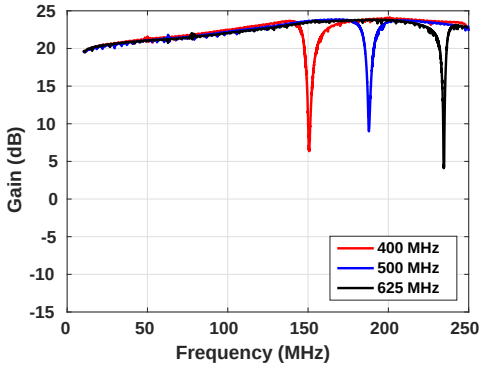
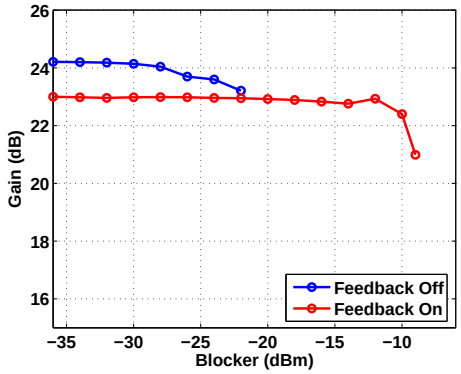
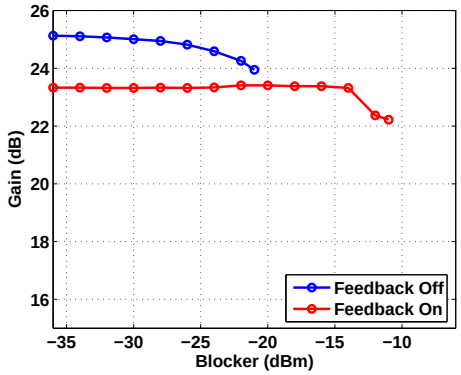


(c)

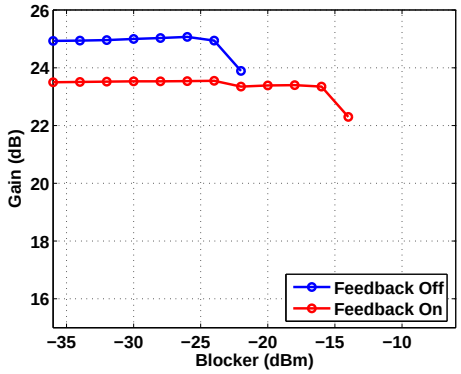
Figure 2.16: The measured notch response for various operating modes of the AFS-HRM, for master clock frequencies from 400-625 MHz (a) f_{LO} mode (b) $2f_{LO}$ mode (c) $3f_{LO}$ mode.



(a)

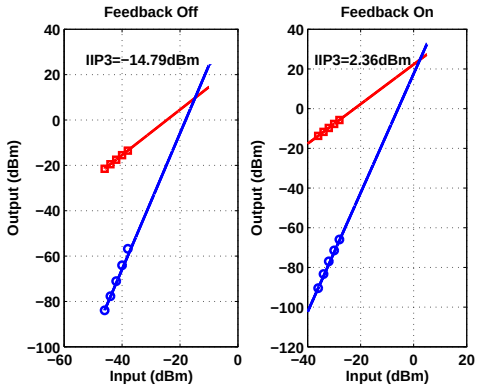


(b)

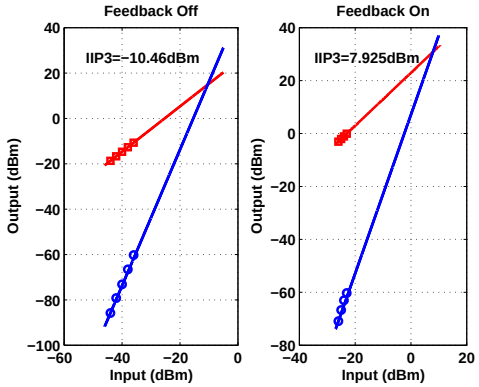


(c)

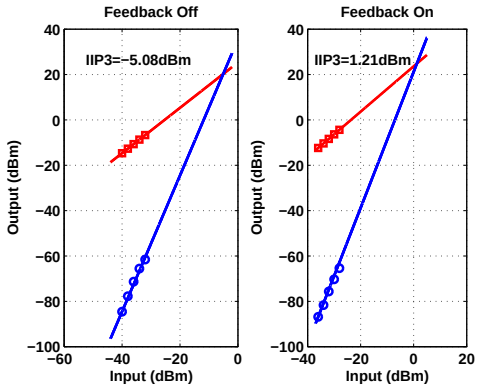
Figure 2.17: Measured blocker 1-dB compression with and without interference cancellation with a blocker at 40 MHz offset (a) f_{LO} mode (b) $2f_{LO}$ mode (c) $3f_{LO}$ mode.



(a)



(b)



(c)

Figure 2.18: IIP3 measurement with and without interference cancellation (a) f_{LO} mode (b) $2f_{LO}$ mode (c) $3f_{LO}$ mode

Table 2.1: Performance summary

Ref	This work	[14]	[16]	[32]
Cancellation method	**Feedback OFF / ON**	Feedforward OFF / ON	Feedback OFF / ON	Feedback OFF / ON
Freq	**0-250MHz**	1.96 GHz	1.9 GHz	2-6 GHz
Gain (dB)	**24.5 / 23**	23.4 / 20.9	24.7 / 22.5	43 / 41
B-1dB CP(dBm)	**-22 / -9**†	-12 / 0	-28 / -17.5	-23 / -16
IIP3(dBm)	**-14.8 / 2.3**†	2.6 / NA	NA	-13 / -5
NF (dB)	**4.5 / 7**	3.9 / 6.8	8.8 / 8.9	3.2 / 5.7
I_{DC} (mA)	**8.33 / 49.8**	8 / 29	150	44 / 56
Supply (V)	**1.2 & 1.4**	1.2 & 2.5	2.5	1.2
Technology	**65nm CMOS**	65nm CMOS	65nm CMOS	65nm CMOS
Harmonic Rejection	**Yes**	No	No	No

†:f_{LO} mode

2.6 Conclusion

An active feedback-based interference cancellation technique is demonstrated. The technique employs harmonic rejection in the down- and up-conversion paths of a feedback loop, to provide a frequency-translated notch response at its input. The frequency span of the synthesizer required for tuning the rejection response is reduced significantly through the generation of fundamental and harmonics of the LO within the harmonic rejection mixers. The design can be employed in broadband radios and spectrum channelizers for providing in-band active interference cancellation.

Chapter 3

LPTV System Analysis with Harmonic Transfer Matrix[1]

3.1 Introduction

Linear systems can be categorized as linear-time-invariant (LTI) and linear-time-varying (LTV) systems. LTI systems are characterized by an impulse response in the time domain and by a frequency response in the frequency domain. The impulse response in these systems depends only on the difference between the application time of the impulse, t_1, and the observation time t_2, and is specified as $h(\tau)$, where $\tau = t_2 - t_1$. There is no frequency translation between the input and the output, and thus the frequency response is given by a function $H(s)$, where $s = j\omega$, is the input frequency.

LTV systems can also be characterized by an impulse response in the time domain and by a frequency response in the frequency domain. However, the impulse response $h(t_2, t_1)$ depends both on the impulse launch time t_1 and the response observation time t_2. Also, since there will, in general, be

[1]Part of the material described in this chapter is based on [27], which was published in the IEEE Radio Frequency Integrated Circuits Symposium, 2015. The author Wei-Gi Ho was responsible for the design, and measurement of the IC described in the publication, and for theoretical analysis of the design.

frequency translation between the input and output, the system frequency response needs to be specified by $H(s_1, s_2)$, where $s_1 = j\omega_1$ represents the input frequency and $s_2 = j\omega_2$ represents the output frequency.

Among various kinds of LTV systems, the linear-periodic-time-varying (LPTV) system is of particular interest in RF communication systems. A frequency translation mixer, for example, can be well modeled as an LPTV system. The impulse response of an LPTV system with fundamental frequency f_{LO} repeats every $T_{LO} = 1/f_{LO}$ in the time domain. In the frequency domain, an LPTV system will translate the input frequency by f_{LO} and its harmonics. In this chapter, harmonic-transfer-matrix based frequency-domain analysis which can be applied to any LPTV system is described.

3.2 Linear Systems

3.2.1 Linear Time-Invariant System

Linear time-invariant (LTI) systems have been extensively studied in literature [33]. The input signal $x(t)$ and the output signal $y(t)$ of an LTI system are related by the convolution integral

$$y(t) = \int_{\tau=-\infty}^{\infty} h(\tau)x(t-\tau)d\tau. \tag{3.1}$$

It can be seen from Eq (3.1) that $y(t)$ is a weighted sum of the input $x(t-\tau)$. The weighting function $h(\tau)$ can be interpreted as the response of the system at time t to an impulse applied at time $t-\tau$. Therefore, $h(t)$ is referred as the impulse response of the system. For a casual system, the output depends only

on the past inputs and $h(\tau) = 0$ for all negative τ. For this case, Eq (3.1) can be written as

$$y(t) = \int_{\tau=0}^{\infty} h(\tau)x(t-\tau)d\tau. \tag{3.2}$$

In the frequency domain, an LTI system is characterized by its response to a complex exponential input e^{st}. By letting $x(\tau) = e^{s\tau}$ in Eq (3.2), after some simplification, we have

$$y(t) = \left\{ \int_{\tau=0}^{\infty} h(\tau)e^{-s\tau}d\tau \right\} e^{st}, \tag{3.3}$$

which implies that for an complex exponential input, e^{st}, the output of the LTI system will be the same complex exponential e^{st} scaled by $H(s)$, where

$$H(s) = \int_{\tau=0}^{\infty} h(\tau)e^{-s\tau}d\tau. \tag{3.4}$$

$H(s)$ is referred as the frequency response of the LTI system, and is the Laplace transform of its impulse response $h(\tau)$.

In summary, an LTI system is completely characterized by its impulse response $h(\tau)$ in the time domain and by its frequency response $H(s)$ in the frequency domain. The frequency response $H(s)$ and the impulse response $h(\tau)$ are related by the Laplace transform, as shown in Eq (3.4). An important property of an LTI system is that it cannot provide any frequency translation, since an input complex exponential e^{st} will simply produce an output complex exponential with the same complex frequency s (Eq (3.3)).

3.2.2 Linear Periodic Time-Varying System

As described in [34], the input and output of a general LTV system can be related by

$$y(t_2) = \int_{t1=-\infty}^{\infty} h(t_2, t_1)x(t_1)dt_1 \tag{3.5}$$

where $x(t_1)$ represents the input at t_1 and $y(t_2)$ represent the output at t_2. The impulse response $h(t_2, t_1)$ represents the response at t_2 due to an impulse applied at t_1. Eq (3.5) can be derived from the superposition principle, which holds for any linear system.

An LPTV system with fundamental frequency f_{LO} is usually referred as a T_{LO}-periodic LPTV system. Its impulse response repeats every $T_{LO} = 1/f_{LO}$. Mathematically, it can be represented as

$$h(t_2 + T_{LO}, t_1 + T_{LO}) = h(t_2, t_1), \quad \forall t_1, t_2 \in \mathbb{R}. \tag{3.6}$$

Eq (3.5) can be re-written as

$$y(t_2) = \int_{\tau=-\infty}^{\infty} h(t_2, t_2 - \tau)x(t_2 - \tau)d\tau. \tag{3.7}$$

Since $h(t_2, t_2-\tau)$ is T_{LO}-periodic in t_2, it can be represented by a Fourier series with fundamental frequency f_{LO}

$$h(t_2, t_2 - \tau) = \sum_{k=-\infty}^{\infty} h_k(\tau)e^{j2\pi k f_{LO} t_2}. \tag{3.8}$$

Substituting Eq (3.8) into Eq (3.7), we have

$$y(t_2) = \sum_{k=-\infty}^{\infty} \int_{\tau=-\infty}^{\infty} h_k(\tau)x(t_2 - \tau)e^{j2\pi k f_{LO} t_2} d\tau. \tag{3.9}$$

Assuming that the input is a complex exponential with complex frequency s, by substituting $x(t_2 - \tau)$ with $e^{s(t_2-\tau)}$, Eq (3.9) becomes

$$\begin{aligned} y(t_2) &= \sum_{k=-\infty}^{\infty} \left[\int_{\tau=-\infty}^{\infty} h_k(\tau) e^{-s\tau} d\tau \right] \times e^{(s+j2\pi k f_{LO})t_2} \\ &= \sum_{k=-\infty}^{\infty} H_k(s) \times e^{(s+j2\pi k f_{LO})t_2}. \end{aligned} \tag{3.10}$$

Eq (3.10) says that a general T_{LO}-periodic LPTV system will frequency translate an input complex exponential with frequency s to an output frequency $s + j2\pi k f_{LO}$ by $H_k(s)$. $H_k(s)$ thus is called the harmonic transfer function between the input frequency s and the output frequency $s + j2\pi k f_{LO}$.

3.3 Harmonic Transfer Matrix Representation of a Linear Periodic Time-Varying System

In the following section, we will first discuss the use of a harmonic transfer matrix to represent an LPTV system. Harmonic transfer matrix representation of an LTI system will be discussed next as a special case of a LPTV system.

3.3.1 Linear Periodic Time-Varying System

From Eq (3.10), a T_{LO}-periodic LPTV system can frequency-translate a complex exponential input with frequency s to output frequencies $s+j2\pi k f_{LO}$. Similarly, an output frequency s, in a T_{LO}-periodic LPTV system, can result from an input at frequencies $s + j2\pi k f_{LO}$. It follows that for a T_{LO}-periodic LPTV system, the input frequencies $s + j2\pi n f_{LO}$ and output frequencies $s +$

$j2\pi m f_{LO}$ are related to each other.

If the input is now represented by a column vector $\widetilde{V_{in}}(s)$

$$\widetilde{V_{in}}(s) = \begin{bmatrix} \vdots \\ V_{in}(s - j\omega_{LO}) \\ V_{in}(s) \\ V_{in}(s + j\omega_{LO}) \\ \vdots \end{bmatrix} \tag{3.11}$$

and the output is represented by a column vector $\widetilde{V_{out}}(s)$

$$\widetilde{V_{out}}(s) = \begin{bmatrix} \vdots \\ V_{out}(s - j\omega_{LO}) \\ V_{out}(s) \\ V_{out}(s + j\omega_{LO}) \\ \vdots \end{bmatrix} \tag{3.12}$$

then the LPTV system can be characterized by a doubly-infinite matrix $\widetilde{\mathbf{H}}(s)$

$$\widetilde{\mathbf{H}}(s) = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & \widetilde{H}_{-1,-1}(s) & \widetilde{H}_{-1,0}(s) & \widetilde{H}_{-1,1}(s) & \cdots \\ \cdots & \widetilde{H}_{0,-1}(s) & \widetilde{H}_{0,0}(s) & \widetilde{H}_{0,1}(s) & \cdots \\ \cdots & \widetilde{H}_{1,-1}(s) & \widetilde{H}_{1,0}(s) & \widetilde{H}_{1,1}(s) & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix} \tag{3.13}$$

where $\widetilde{\mathbf{H}}(s)$ is called the Harmonic Transfer Matrix (HTM) representation of the LTPV system [35][36]. The HTM provides a compact representation of an LPTV system. It is useful for calculating the harmonic transfer function of such a system.

Using Eq (3.11) (3.12) and (3.13), the input and output relationship of

a LPTV system can be written as

$$\widetilde{V_{out}}(s) = \widetilde{\mathbf{H}}(s)\widetilde{V_{in}}(s). \tag{3.14}$$

It follows that $\widetilde{H}_{m,n}(s)$ is the transfer function that will frequency translate an input at $s + j2\pi n f_{LO}$ to an output at $s + j2\pi m f_{LO}$. This is graphically represented in Fig. 3.1.

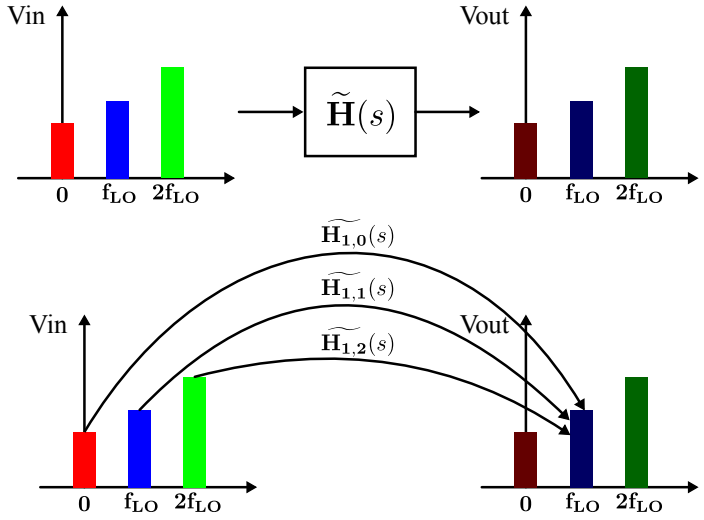


Figure 3.1: Transfer function between the input and the output in different bands represented by the element of the corresponding HTM

In practical applications, the size of $\widetilde{\mathbf{H}}(s)$ is usually truncated such that the elements that are sufficiently small are neglected.

3.3.2 Linear Time-Invariant System

As discussed in Sec. 3.2.1, an LTI system cannot provide any frequency translation. It follows that if the input and output are specified by the column

vectors shown in Eq (3.11) and (3.12), respectively, the HTM of an LTI system can be represented by

$$\widetilde{\mathbf{H}}(s) = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & H_0(s - j\omega_{LO}) & 0 & 0 & \cdots \\ \cdots & 0 & H_0(s) & 0 & \cdots \\ \cdots & 0 & 0 & H_0(s + j\omega_{LO}) & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix}. \tag{3.15}$$

This is a diagonal matrix, since there is no frequency translation in an LTI system.

3.3.3 Properties of the Harmonic Transfer Matrix

Given a system containing both LPTV and LTI sub-systems, each represented by its corresponding HTM, the HTM of the system can be represented by the HTMs of the individual sub-systems.

An important property of a HTM is that if a system is composed of cascade of LTI and LPTV sub-systems, then the HTM representation of the composite system is the product of the individual HTM's representing the sub-systems. The order of the HTM's product is the same as the order in which the sub-systems are cascaded. This is illustrated in Fig. 3.2.

3.4 Applications of HTM-based Analysis

3.4.1 Tunable High-Q Bandpass Filter

A switched-RC 4-path filter with a band-pass characteristic is proposed in [19]. An analysis of its operation based on a state-space methodology is also

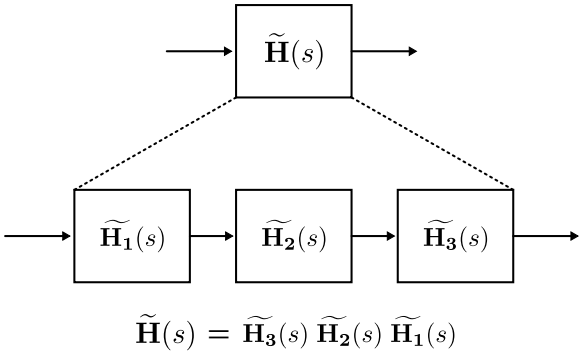


Figure 3.2: Cascade of sub-systems represented by individual HTMs and the equivalent HTM representation for the composite system

described. Since it is an LPTV system, an HTM-based analysis can also be employed. The 4-path BPF is shown in Fig. 3.3. If H_k denotes the HTM of

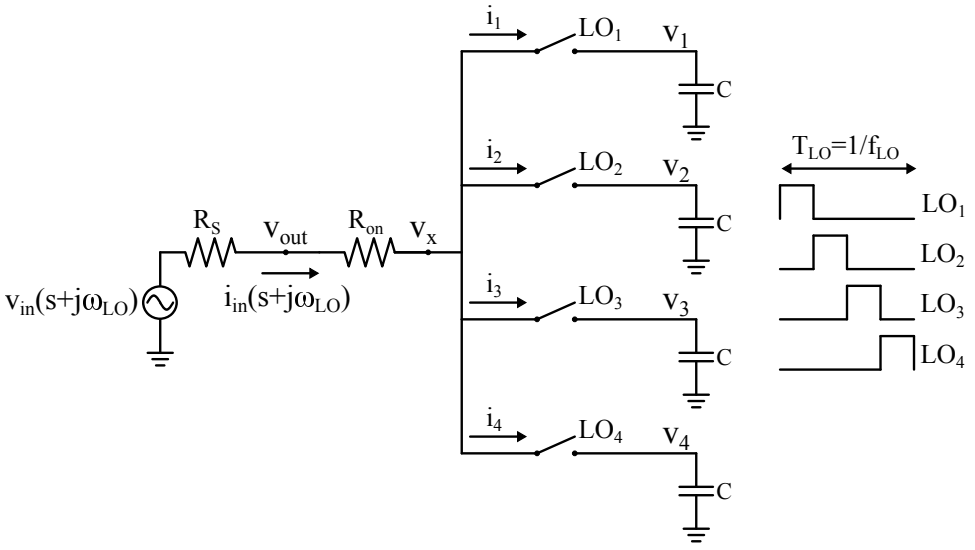


Figure 3.3: A switched RC 4-path BPF

an LPTV system that multiplies the input with LO_k, for k = 1-4, the current

i_k can be written as

$$i_k = H_k i_{in} \tag{3.16}$$

with H_k given by

$$H_k = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & a_0 & a_{-1}e^{\frac{j2\pi}{4}(k-1)} & a_{-2}e^{\frac{j2\pi}{4}2(k-1)} & \cdots \\ \cdots & a_1 e^{\frac{-j2\pi}{4}(k-1)} & a_0 & a_{-1}e^{\frac{j2\pi}{4}(k-1)} & \cdots \\ \cdots & a_2 e^{\frac{-j2\pi}{4}2(k-1)} & a_1 e^{\frac{-j2\pi}{4}(k-1)} & a_0 & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix} \tag{3.17}$$

where the coefficients $a_n's$ are given by

$$a_n = \frac{1}{4} sinc\left(\frac{n}{4}\right) \tag{3.18}$$

and represent the n^{th} Fourier series coefficient of LO_1.

The capacitor voltages v_k can be expressed as

$$v_k = Z_C i_k = Z_C H_k i_{in}, \tag{3.19}$$

where Z_C is the HTM of the impedance of the capacitor C

$$Z_C = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & \frac{1}{(s-j\omega_{LO})C} & 0 & 0 & \cdots \\ \cdots & 0 & \frac{1}{sC} & 0 & \cdots \\ \cdots & 0 & 0 & \frac{1}{(s+j\omega_{LO})C} & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix}. \tag{3.20}$$

Since node v_x is connected to v_k when LO_k is high, the voltage v_x can be

represented as

$$\begin{aligned} v_x &= H_1 v_1 + H_2 v_2 + H_3 v_3 + H_4 v_4 \\ &= (H_1 Z_C H_1 + H_2 Z_C H_2 + H_3 Z_C H_3 + H_4 Z_C H_4) i_{in} \end{aligned} \tag{3.21}$$

Applying KCL, we have

$$v_{in} - i_{in}(R_S + Ron) = (H_1 Z_C H_1 + H_2 Z_C H_2 + H_3 Z_C H_3 + H_4 Z_C H_4) i_{in}. \tag{3.22}$$

As shown in the Appendix-A, by assuming that the input signal v_{in} is at a frequency close to ω_{LO} and the only non-zero element in Z_C is $\frac{1}{sC}$, Eq (3.22) can be solved for $i_{in}(s + j\omega_{LO})$

$$i_{in}(s + j\omega_{LO}) = \frac{v_{in}(s + j\omega_{LO})}{R_S + R_{on}} \frac{(|a_3|^2 + |a_5|^2 + ...)\frac{4}{sC(R_S + R_{on})}}{1 + (|a_1|^2 + |a_3|^2 + |a_5|^2 + ...)\frac{4}{sC(R_S + R_{on})}}. \tag{3.23}$$

For the $a_n's$ given by Eq (3.18), it can be shown that

$$|a_1|^2 + |a_3|^2 + |a_5|^2 + ... = \frac{1}{16} \tag{3.24}$$

$$|a_3|^2 + |a_5|^2 + ... = \frac{1}{16}\left(1 - \frac{8}{\pi^2}\right). \tag{3.25}$$

Combing Eq (3.23) (3.24) and (3.25), we have

$$i_{in}(s + j\omega_{LO}) = \frac{v_{in}(s + j\omega_{LO})}{R_S + R_{on}} \frac{(1 - \frac{8}{\pi^2})\frac{1}{4sC(R_S + R_{on})}}{1 + \frac{1}{4sC(R_S + R_{on})}}. \tag{3.26}$$

Similar to [19], an equivalent RLC model for this band-pass filter around ω_{LO} can be derived by matching the input current i_{in} for small s in Fig. 3.3

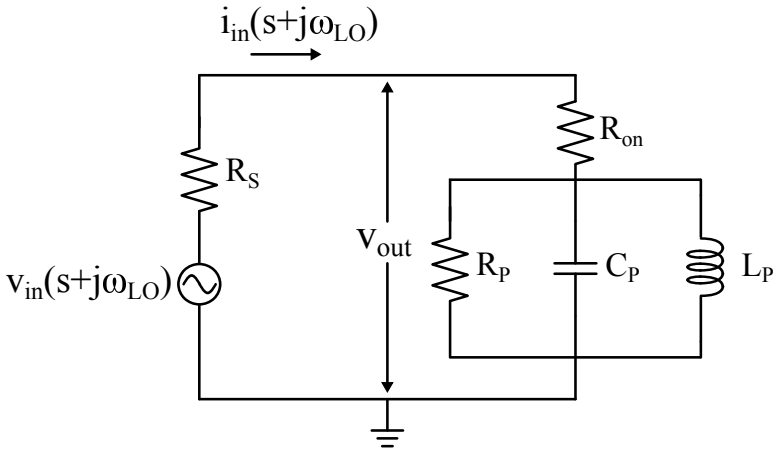


Figure 3.4: An equivalent RLC model for the 4-path BPF

and Fig. 3.4, we have

$$R_p = (R_s + R_{on})\frac{8}{\pi^2 - 8} \tag{3.27}$$

$$C_p = 2\frac{R_s + R_{on} + R_p}{R_s + R_{on}}C \tag{3.28}$$

$$L_p = \frac{1}{\omega_{LO}^2 C_p}. \tag{3.29}$$

To verify the equivalence between the 4-path BPF and the equivalent RLC network, simulation is performed in Cadence SpectreRF for the two circuits. Parameters $\omega_{LO} = 2\pi \times 500\, Mrad/sec$, $C = 100\, pF$, $R_S = 50\,\Omega$ and $R_{on} = 10\,\Omega$ are used for the 4-path BPF, and the corresponding $R_p = 256.74\,\Omega$, $C_p = 246.74\, pF$ and $L_p = 410.64\, pH$, as calculated from Eq (3.27)-(3.29), are used for its equivalent RLC model. The simulated responses at v_{out} are compared and the result is shown in Fig. 3.5. It can be seen that the responses

match very closely around ω_{LO}.

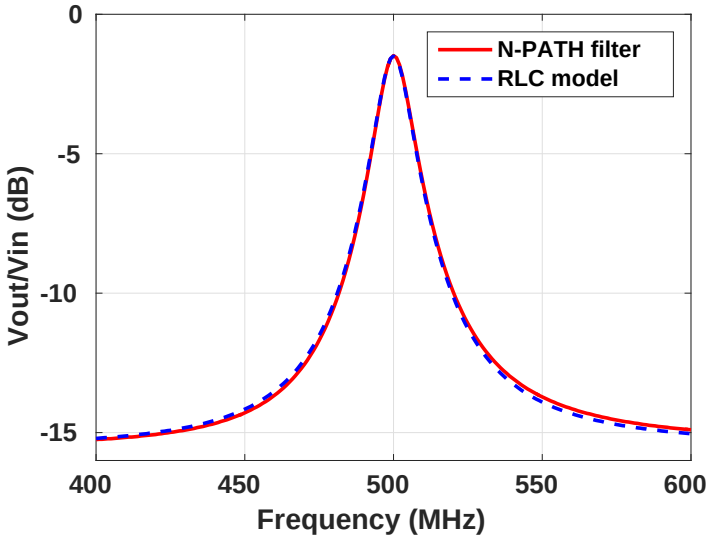


Figure 3.5: The simulated response at v_{out} for the 4-path BPF and its equivalent RLC model

3.4.2 The Proposed Interferer Canceler

The Harmonic Transfer Matrix for an AFS-HRM discussed in Sec. 2.3 can be written as

$$\widetilde{\mathbf{H}}(s) = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & A_0 & A_{-1} & A_{-2} & \cdots \\ \cdots & A_1 & A_0 & A_{-1} & \cdots \\ \cdots & A_2 & A_1 & A_0 & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix}, \tag{3.30}$$

where A_i represents the i^{th} Fourier series coefficient of the equivalent down-conversion LO waveform. Depending on different operating modes, the coefficients in $\widetilde{\mathbf{H}}(s)$ will assume different values. For example, in the f_{LO} mode,

except for $A_{\pm 1}$, $A_{\pm 7}$ and $A_{\pm 9}$ ..., all other elements will be ideally zero. These are in fact the amplitudes of the non-zero harmonics that are contained in the discrete sine-wave LO that is synthesized at f_{LO} within the HRM. In practice, due to the presence of non-ideal gain coefficients in the implementation, other coefficients will be non-zero, although small. In the following discussion, we will assume that these small coefficients can be neglected in the HTM. In $3f_{LO}$ mode, on the other hand, $A_{\pm 3}$, $A_{\pm 5}$ and $A_{\pm 11}$ .... will be the significant terms. The maximum achievable rejection of the proposed interference canceler and the harmonic folding phenomena are discussed below.

3.4.3 Analysis of the AFS-HRM Based Interference Canceler

3.4.3.1 Maximum Achievable Rejection

We analyze below the maximum rejection that can be provided by the canceler, taking into consideration the presence of finite harmonics in the HRMs used in Fig. 2.4.

The HTM for the q^{th} path of the down-conversion AFS-HRM can be written as

$$\widetilde{H^{q}_{down}}(s) = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & A_0 & A_{-1}e^{jq\times 45^o} & A_{-2}e^{jq\times 90^o} & \cdots \\ \cdots & A_1 e^{-jq\times 45^o} & A_0 & A_{-1}e^{jq\times 45^o} & \cdots \\ \cdots & A_2 e^{-jq\times 90^o} & A_1 e^{-jq\times 45^o} & A_0 & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix} \tag{3.31}$$

for $q = 1 : 8$. In the above matrix, we note that the fundamental frequency-translation term in path q is scaled by the coefficient A_{-1} and includes a

phase-shift of $q \times 45°$. The phase-shift arises due to the phase-shift of the master clock that is applied to the individual paths (Fig. 2.5).

The up-conversion AFS-HRM has an HTM which is identical to that of the down-conversion AFS-HRM

$$\widetilde{H^q_{up}}(s) = \widetilde{H^q_{down}}(s).$$

If the HTM of the baseband filter is represented by $\widetilde{H_{BB}}(s)$, from Fig. 2.4, we have

$$AV_{in}(s) - \sum_{q=1}^{8} \widetilde{H^q_{up}}(s)\widetilde{H_{BB}}(s)\widetilde{H^q_{down}}(s) \times V_{out}(s) = V_{out}(s). \tag{3.32}$$

As shown in the Appendix-B, by assuming that the BB-LPF has sufficient attenuation for frequencies greater than f_{LO}, the in-band component $V_{out}(s + jk\omega_{LO})$ can be solved for different operating modes (kf_{LO} mode) of the AFS-HRM. If the AFS-HRM is operating in the f_{LO} mode, we have

$$\begin{aligned} V_{out}(s + j\omega_{LO}) = &\left\{ \frac{1 + H_0(s)(|A_7|^2 + |A_9|^2 + ...)}{1 + H_0(s)(|A_1|^2 + |A_7|^2 + |A_9|^2 + ...)} \right\} \\ &\times AV_{in}(s + j\omega_{LO}). \end{aligned} \tag{3.33}$$

The maximum in-band achievable rejection for the f_{LO} mode is

$$R_1 \approx \frac{|A_7|^2 + |A_9|^2 + ...}{|A_1|^2 + |A_7|^2 + |A_9|^2 + ...}.$$

since $H_0(s)(|A_1|^2 + |A_7|^2 + |A_9|^2 + ...) \gg 1$ and $H_0(s)(|A_7|^2 + |A_9|^2 + ...) \gg 1$. For the $A'_k s$ given by Eq (2.8), by using the Parseval's equality, it can be shown

that

$$|A_1|^2 + |A_7|^2 + |A_9|^2 + ... = 1,$$

hence

$$R_1 = 1 - \left\{ \frac{sin\left(\frac{\pi}{8}\right)}{\frac{\pi}{8}} \right\}^2 \approx -26\ dB.$$

The above result provides us with the theoretical limit on rejection that can be achieved in an HRM-based N-path filter placed inside a feedback loop, to synthesize a null.

Similarly, if the input is now around other harmonics, say $3f_{LO}$, and the AFS-HRMs are still operating in f_{LO} mode, we have

$$V_{out}(s + j3\omega_{LO}) = \left\{ \frac{1 + H_0(s)(|A_5|^2 + |A_{11}|^2 + ...)}{1 + H_0(s)(|A_3|^2 + |A_5|^2 + |A_{11}|^2 + ...)} \right\} \times AV_{in}(s + j3\omega_{LO}). \quad (3.34)$$

In the f_{LO} mode, even in the presence of non-ideal gains, the AFS-HRM can provide a harmonic rejection better than 30 dB. Coefficients $|A_3|$, $|A_5|$, and $|A_{11}|$, ... are thus all small numbers[2]. The combination of AFS-HRMs in the down-conversion and up-conversion paths provides harmonic suppression performance which is similar to a 2-stage harmonic rejection mixer [9] since the harmonic content is proportional to $|A_3|^2$, $|A_5|^2$, $|A_{11}|^2$..., as can be seen from Eq (3.34). The coefficients $|A_3|^2$, $|A_5|^2$, $|A_{11}|^2$ ... are typically about 60 dB smaller than $|A_1|^2$. From Eq (3.33), the baseband filtering $H_0(s)$

[2]Even harmonics are rejected due to differential symmetry

can be chosen to have sufficiently large gain, e.g., 40 dB, to ensure adequate suppression of an interferer around f_{LO}. For signals around $3f_{LO}$, the term $H_0(s)(|A_3|^2 + |A_5|^2 + |A_{11}|^2 + ...)$ will be of the order of 40 dB-60 dB=-20 dB, which is still much less than 1, and therefore no significant attenuation will be observed for an input around $3f_{LO}$, as can be seen from Eq (3.34). The notch seen at V_{out} in Fig. 2.4 thus does not provide significant attenuation at harmonics, unlike in a switch-based N-path filter.

Another way of viewing the equivalent 2-stage harmonic rejection of the proposed architecture is by assuming that the residual harmonic responses of the down-conversion and up-conversion AFS-HRM due to non-ideal harmonic rejection are δ_1 and δ_2, respectively. The signal around say $3f_{LO}$, will be down-converted to baseband with a scaling factor of δ_1 and then up-converted by δ_2. It follows that the total residue response will hence be proportional to $\delta_1\delta_2$.

When the AFS-HRMs are operating in $3f_{LO}$ mode, from Eq (3.34), the maximum achievable rejection is

$$R_3 = \frac{|A_5|^2 + |A_{11}|^2 + ...}{|A_3|^2 + |A_5|^2 + |A_{11}|^2 + ...},$$

which is around -9 dB. This is degraded compared to the f_{LO} mode since $|A_5/A_3| > |A_7/A_1|$. A 2-stage up-conversion scheme proposed in [37] can be used in this case to enhance the rejection, if required by the application.

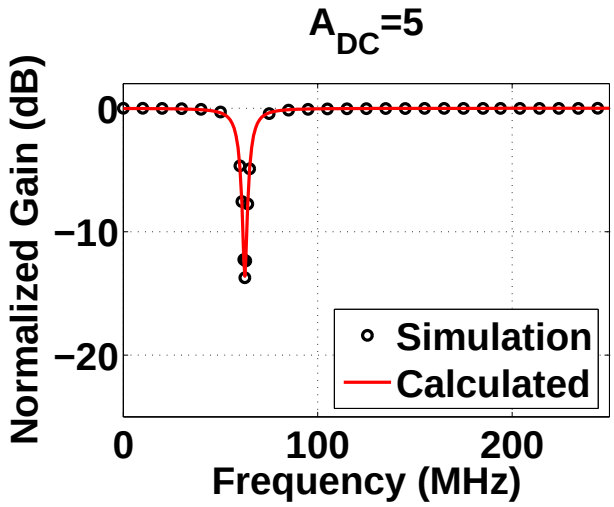
It should be noted from Eq (3.33) and Eq (3.34) that if the out-of-band responses from A_7, A_9, ... in the f_{LO} mode and A_5, A_{11}, ... in the $3f_{LO}$ mode are suppressed, the achievable rejection can be improved. This filter is used

in the combining TIA as described in Sec. 2.4.3.

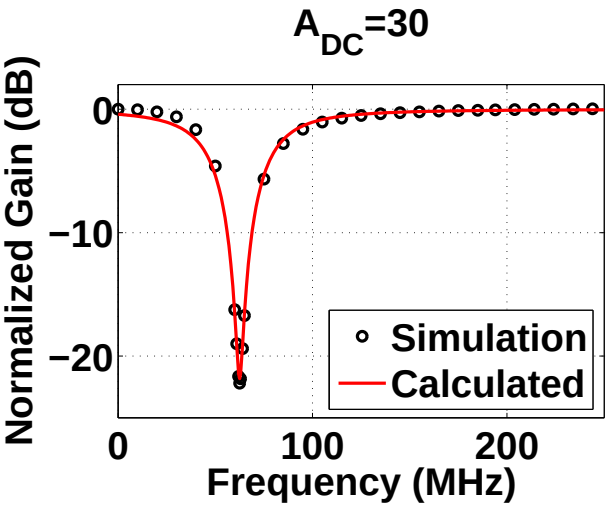
In order to verify the above derivation, Eq (3.33) is compared with simulation result from Cadence SpectreRF. We assume that $H_0(s) = A_{DC}/(1+sRC)$, with $R = 10k\Omega$, $C = 25pF$, where A_{DC} takes two different values, namely 5 and 30. The result is shown in Fig. 3.6. It can be seen that the simulation agrees with theory. The small discrepancy for large A_{DC} can be attributed to the fact that terms other than $H_0(s)$ in the BB-LPF HTM $\widetilde{H_{BB}}(s)$ cannot be entirely neglected. For example, the interferer around f_{LO} may be up-converted to $2f_{LO}$ first, filtered by $H_0(s + j2\omega_{LO})$, and then down-converted back to f_{LO}. Such frequency translation is neglected in the above calculation due to the fact that the baseband filter response $H_0(s + j2\omega_{LO})$ is assumed to be small at frequency $2f_{LO}$. It is also possible to widen the bandwidth of the rejected signal by using a high-order LPF within the loop. However, it is important to make sure that the phase-margin of the loop is not unacceptably degraded, which can be ensured through the use of appropriately placed zeros in the filter transfer function [37].

3.4.3.2 Harmonic Folding

The use of N-path filtering also helps to minimize harmonic folding. Harmonic folding refers to the transfer of signal from its frequency to frequencies around harmonics of the LO. This is important to consider for large interferers, since we want to ensure that while the interferer is suppressed at its original frequency, it does not appear through frequency-translation in the



(a)



(b)

Figure 3.6: Simulated and calculated response using Eq (3.33) for different A_{DC}. (a) $A_{DC} = 5$ (b) $A_{DC} = 30$

loop at other in-band frequencies.

It can be shown that this is not a problem for the architecture, since for an input frequency f_{in}, the first folded harmonic can be shown to be at $f_{in} - Nf_{LO}$. Thus if $N = 8$ paths are used and the input bandwidth is $4f_{LO}$, then all the harmonic folding terms will fall out-of-band.

In order to prove this, consider the following sum

$$S = \sum_{q=1}^{8} \widetilde{H_{up}^{q}}(s)\widetilde{H_{BB}}(s)\widetilde{H_{down}^{q}}(s). \tag{3.35}$$

The $s_{u,v}$ element in the S matrix that will frequency-translate $V_{in}(s + jv\omega_{LO})$ to $V_{out}(s + ju\omega_{LO})$ can be computed as

$$s_{u,v} = \left\{ \sum_{q=1}^{8} e^{j(u-v)q\times 45^{o}} \right\} \times \left\{ \sum_{r=-\infty}^{\infty} A_{u-v-r} H_{BB}(s + j(v + r)\omega_{LO}) A_r \right\} \tag{3.36}$$

and it will be zero except for $u - v = 8\mathbb{Z}$ because the existence of the first term $\sum_{q=1}^{8} e^{j(u-v)q\times 45^{o}}$. Thus if the bandwidth is limited to $4f_{LO}$, by using 8 paths the unwanted harmonic foldings will ideally all appear outside the bandwidth of the input signal. In practice, non-ideal matching will result in the phase shift among the 8 paths being not equal to 45°, hence causing residual non-zero harmonic folding from the input frequency to other in-band frequencies. The key source of the mismatch will be the mismatch amongst the phase response of the BB-LPFs, which is a 2^{nd}-order effect. Phase mismatches in the clocking errors amongst the 8 paths are effectively eliminated by the re-timing technique as described Chapter 2.

3.5 Conclusion

In this chapter, the representation of LPTV systems by HTMs is discussed. This technique allows LPTV systems to be analyzed using traditional circuit analysis methodology such as nodal analysis, in a manner similar to LTI systems. Application of the HTM approach to the analysis of an N-path BPF and the proposed interference canceler is presented. The resulting linear system can be solved by using a signal flow graph and Mason's gain rule, which gives greater design insight into the circuit. The solution obtained by using the HTM technique shows good agreement with the simulation results.

Chapter 4

A Bias-Shared Two-Stage Harmonic Rejection Mixer[1]

4.1 Introduction

Receivers with broadband signal inputs are typically required to downconvert a desired portion of the spectrum around the local oscillator (LO) frequency while avoiding downconversion from all LO harmonics. Ideal rejection of all LO harmonics requires the use of a multiplier with a sinusoidal LO. Practical mixers however amplitude-limit the LO signal, in order to make the gain independent of the LO amplitude and reduce SNR degradation due to LO amplitude noise. For instance, a current-commutating mixer internally converts a sinusoidal LO to a waveform that approximates a square-wave LO with a 50% duty cycle. In this case, the n^{th} odd harmonic has a relative amplitude of $1/n$ compared to the fundamental, and can lead to significant spurious downconversion.

Harmonic-rejection mixers (HRMs) first proposed in [8] can be used to downconvert broadband signals while mitigating folding of unwanted signals

[1]Part of the material described in this chapter is based on [40], which was published in the IEEE Midwest Symposium on Circuits and Systems (MWSCAS), 2015. The author Wei-Gi Ho was responsible for the design, and measurement of the IC described in the publication, and for theoretical analysis of the design.

from harmonics of the downconversion LO. These mixers use linear combinations of a two-level periodic switching basis waveform, in order to synthesize a discrete approximation to a sine-wave LO [23], thus rejecting specific harmonics of the LO. HRMs retain the advantage of switching mixers with regards to insensitivity to LO amplitude, unlike multipliers with sinusoidal LOs.

Two-stage harmonic rejection mixers have been demonstrated to provide excellent harmonic rejection performance, by desensitizing the design to gain coefficient and clock timing errors [9][11]. These HRMs use two single-stage HRMs, implemented using RF and baseband gain-coefficients, where each stage requires its own bias current.

In this work, we demonstrate the use of bias-current reuse in a two-stage 8-phase HRM with clock-retiming, to reduce power dissipation. The 1^{st}-stage of harmonic rejection is provided by NMOS transconductors that operate at RF. The RF current from this stage is commutated through passive mixer switches that employ clock re-timing, downconverted to baseband, and applied to common-gate (CG) devices that serve as trans-impedance amplifiers. The CG outputs are applied to PMOS loads that are used to bias the NMOS transconductors. The PMOS load devices are configured as common-source amplifiers, and provide the 2^{nd}-stage of harmonic rejection. The design operates as a direct-downconversion receiver, and provides quadrature outputs at baseband.

The basic principle of operation of the architecture is described in Sec. 4.2. Circuit-level description of the architecture is provided in Sec. 4.3. Perfor-

mance of the bias-shared 2-stage HRM, including its harmonic rejection ratio, noise and linearity, is discussed in Sec. 4.4. Specific challenges that arise from the use of bias-reuse, including flicker noise and potential degradation in harmonic rejection are described and solutions are proposed. Measurement results are provided in Sec. 4.5 and conclusions in Sec. 4.6.

4.2 A Two-Stage Harmonic Rejection Mixer with Bias-Current Reuse

4.2.1 Two-Stage Harmonic Rejection Principle

As discussed in Chapter-2, an 8-path HRM with ideal gain coefficients completely rejects the 3^{rd} and 5^{th} harmonics. For $N = 8$, the non-zero coefficients are scaled with relative magnitudes of $1 : \sqrt{2} : 1$. In a practical implementation, an integer ratio approximation is used since it can be implemented easily using device scaling. Two commonly used approximate integer ratios include $2 : 3 : 2$ and $5 : 7 : 5$. If the integer ratio is written as $1 : \sqrt{2} + \delta_a : 1$, the 3^{rd} and 5^{th} harmonics of the synthesized sinusoidal will have error component LO_3 and LO_5

$$\begin{aligned} LO_3 &= \frac{2}{8} sinc\left(\frac{3}{8}\right) \left\{1 + (\sqrt{2} + \delta_a)e^{-j135^o} + e^{-j270^o}\right\} \\ &= \frac{2}{8} sinc\left(\frac{3}{8}\right) \delta_a e^{-j135^o} \end{aligned} \tag{4.1}$$

$$\begin{aligned} LO_5 &= \frac{2}{8} sinc\left(\frac{5}{8}\right) \left\{1 + (\sqrt{2} + \delta_a)e^{-j225^o} + e^{-j450^o}\right\} \\ &= \frac{2}{8} sinc\left(\frac{5}{8}\right) \delta_a e^{-j225^o} \end{aligned} \tag{4.2}$$

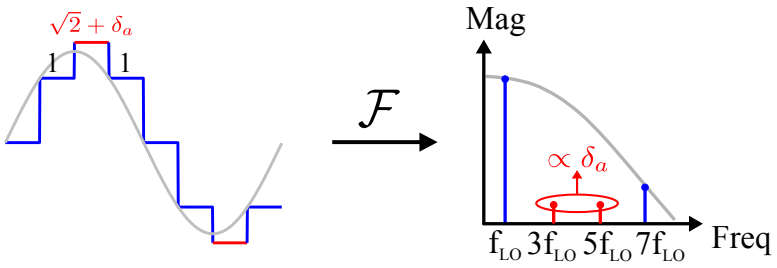


Figure 4.1: Impact of amplitude error δ_a on the 3^{rd} and 5^{th} harmonics of f_{LO}

In such a case, the effective LO has an error term which is proportional to δ_a. Random variations also contribute to this error. This error introduces harmonic content proportional to δ_a and degrades the harmonic rejection, as illustrated in Fig. 4.1.

An approach to mitigate the impact of errors arising from non-ideal gain coefficients based on the use of two-stage harmonic rejection was described in [9]. A block-level implementation of the design is shown in Fig. 4.2. The effective LOs that operate on the input are synthesized using a first stage of gains that approximate $1 : \sqrt{2} : 1$. The 1^{st}-stage gains are applied to the RF signal, and can be implemented using low-noise transconductance amplifiers (LNTAs). The RF input is downconverted to baseband and sequenced into the nodes BB_1-BB_3, using time-offset LO waveforms. The effective downconversion LO that is applied to the signal appearing at each of the nodes is phase-shifted relative to the adjacent nodes by a fixed amount (e.g., $T_{LO}/8$ in Fig. 4.2). The 2^{nd}-stage gains also approximate $1 : \sqrt{2} : 1$, but are applied at baseband. These can potentially be implemented using current-amplifiers, followed by a current-to-voltage conversion. Combination of the paths at base-

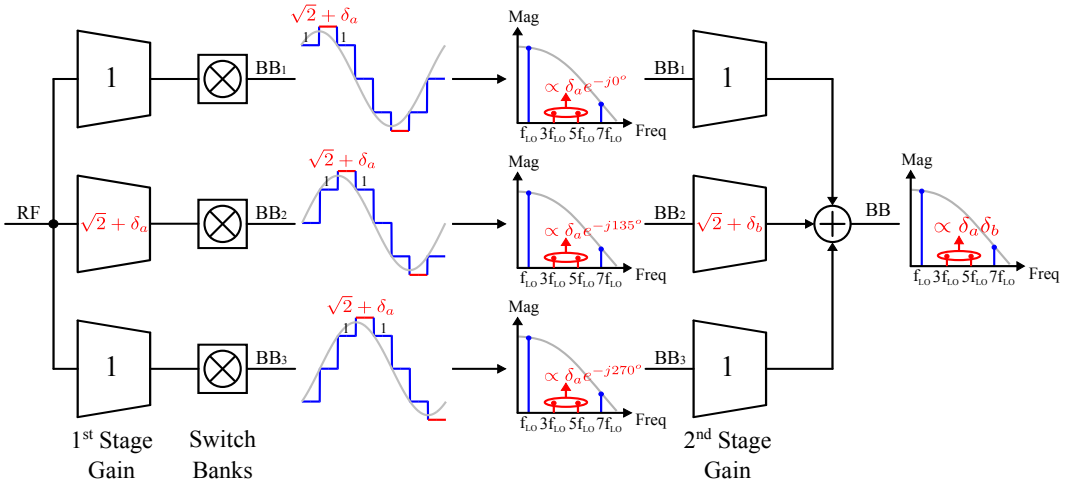


Figure 4.2: Block diagram of a 2-stage HRM

band provides the second stage of harmonic suppression. A more rigorous mathematical description is given below.

If the gain ratios in the 1^{st}-stage are $1 : \sqrt{2}+\delta_a : 1$, the 3^{rd} harmonic component of the LO, LO_3, will downconvert a signal around $3f_{LO}$ to baseband. The strength of the signal at the nodes BB_1-BB_3, relative to the component downconverted by f_{LO}, can be shown to be

$$\begin{aligned} BB_1(LO_3) &= \frac{2}{8} sinc\left(\frac{3}{8}\right)\left\{e^{j135^o} + (\sqrt{2}+\delta_a) + e^{-j135^o}\right\} \\ &= \frac{2}{8} sinc\left(\frac{3}{8}\right)\delta_a e^{-j0^o} \end{aligned} \tag{4.3}$$

$$\begin{aligned} BB_2(LO_3) &= \frac{2}{8} sinc\left(\frac{3}{8}\right)\left\{e^{-j0^o} + (\sqrt{2}+\delta_a)e^{-j135^o} + e^{-j270^o}\right\} \\ &= \frac{2}{8} sinc\left(\frac{3}{8}\right)\delta_a e^{-j135^o} \end{aligned} \tag{4.4}$$

$$BB_3(LO_3) = \frac{2}{8} sinc\left(\frac{3}{8}\right)\left\{e^{-j135^o} + (\sqrt{2}+\delta_a)e^{-j270^o} + e^{-j405^o}\right\}$$
$$= \frac{2}{8} sinc\left(\frac{3}{8}\right)\delta_a e^{-j270^o} \quad (4.5)$$

The final baseband output BB is obtained by combing BB_1-BB_3 and multiplying with the 2^{nd}-stage gain coefficients, which are assumed to have the ratio of $1 : \sqrt{2}+\delta_b : 1$. We then have

$$BB(LO_3) = BB_1(LO_3) + (\sqrt{2}+\delta_b)BB_2(LO_3) + BB_3(LO_3)$$
$$= \frac{2}{8} sinc\left(\frac{3}{8}\right)\delta_a\left\{1 + (\sqrt{2}+\delta_b)e^{-j135^o} + e^{-j270^o}\right\}$$
$$= \frac{2}{8} sinc\left(\frac{3}{8}\right)\delta_a\delta_b e^{-j135^o}. \quad (4.6)$$

Form Eq (4.6), we can see that if the 1^{st}-stage has a coefficient error of δ_a and the 2^{nd}-stage an error of δ_b, the net harmonic rejection in the final baseband output BB is proportional to $\delta_a\delta_b$ [9]. The rejection for the 5^{th} harmonic can also be shown to be proportional to $\delta_a\delta_b$ in a similar fashion. In practical designs, if each stage can provide 30 dB rejection, which is typical without calibration, then the combined output can have a 60 dB rejection without calibration.

4.2.2 Clock Re-timing

The 2-stage harmonic rejection technique desensitizes the design to gain errors. However the HRR is still sensitive to clock phase-errors, such as duty cycle variations in the phase clocks p_k. This is illustrated in Fig. 1.9. An approach for reducing phase sensitivity in a single-stage N-phase active

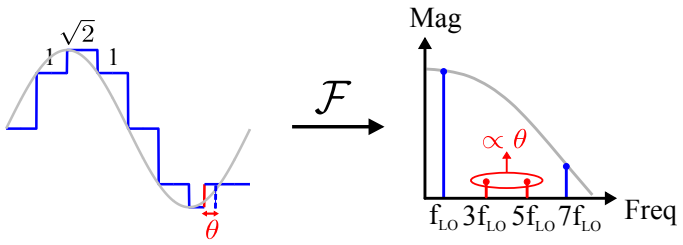


Figure 4.3: Impact of relative clock phase error on HRR

HRM, based on re-timing of clocks by employing a primary clock at f_s, where $f_s = Nf_{LO}$, was shown in [10]. A re–timing approach within a two-stage passive HRM was demonstrated in [11]. It employs the down-conversion switch bank shown in Fig. 2.8 to desensitize the phase-clock errors. For a relative clock phase error of θ on one of the clock paths, the 1^{st}-stage of the HRM will give an HRR proportional to $sin(\theta)$ (Fig. 4.3). After weighted summing in the 2^{nd}-stage gain, with gain-coefficient error δ_b, the net HRR from mf_{LO} was observed to be related to $ksin(\theta)\delta_b$, where k is a scaling constant [38].

4.2.3 Bias-Current Reuse in a Two-Stage HRM

The two-stage HRM (Fig. 4.2) described above requires power dissipation in two gain stages, e.g., for providing the 1^{st}-stage and 2^{nd}-stage gain coefficients, before and after downconversion respectively. The two stages provide gain at different frequencies. It is thus possible to share the bias current between these stages. Furthermore, it is possible to accomplish this without splitting the voltage domains between the RF and baseband amplifiers, such that the RF devices appear as loads for the baseband, and vice versa [39].

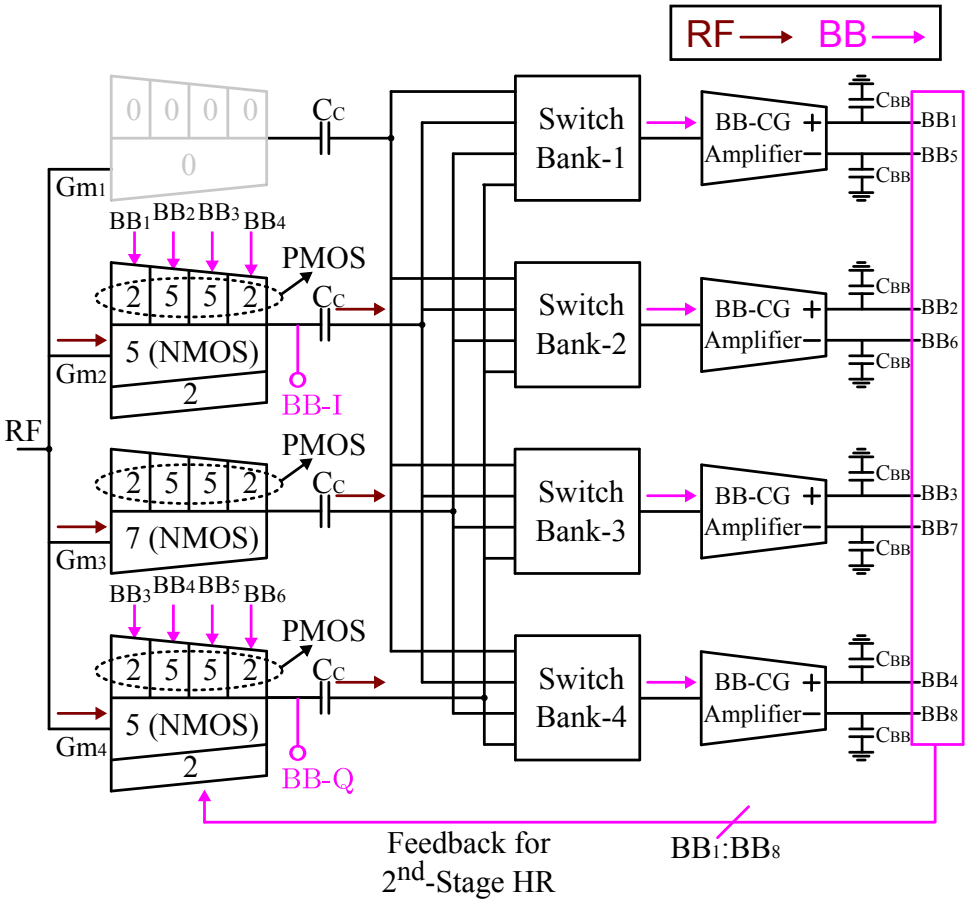


Figure 4.4: Block diagram of a bias-sharing 2-stage HRM

Fig. 4.4 shows the proposed bias-shared 2-stage HRM architecture, with single-ended RF input for clarity [40]. The transconductors Gm_1-Gm_4, consisting of NMOS devices and PMOS devices share the same bias current. These are used to implement both the 1^{st}-stage and 2^{nd}-stage gain ratios. NMOS input devices are used to approximate a sine-wave using G_m-ratios of $0:5:7:5:0:-5:-7:-5$ in an eight-phase HRM configuration. The gain coefficients 0 do not require a G_m-cell. Positive and negative coefficients can

be derived from a single differential transconductance cell. Thus in total three G_m-cells are required. All G_m-cells are designed to contain the same number of NMOS G_m-units, which is nominally set at 7. In two of the three G_m-cells only 5 NMOS G_m-units are used, while all the NMOS G_m-units are used in one of the cells. These cells are termed 5-cell and 7-cell, respectively. The 5-cells use the two NMOS G_m-units as dummies. In this way, the total area of the 5-cells is made identical to that of the 7-cells. This ensures that the ratio of the RF-to-baseband device size stays constant for the 5-cells and the 7-cell. It also ensures that the effective output resistance of the 5-cells and the 7-cell is identical when viewed from the drains. This provides the benefit that the 1^{st}-stage harmonic rejection is not affected by the uncertainty of the device finite output resistance.

The outputs of the RF transconductors are capacitively coupled to the switch banks. These down-convert the RF transconductor currents to baseband, where they are connected to low-impedance source nodes of baseband common-gate (BB-CG) amplifiers (Fig. 4.4). A 1^{st}-stage of harmonic suppression is achieved at nodes BB_1 through BB_8. By phase-shifting the downconversion clocks, e.g., [11], the relative phase shift between $BB_1, BB_2 \cdots BB_8$ is 45^o, as illustrated in Fig. 4.5. It is noted that even in the presence of gain and phase errors, which are shown in red in Fig. 4.5, this 45^o phase relation is still maintained in BB_1-BB_8. This is essential for the effectiveness of the 2^{nd}-stage harmonic rejection.

The outputs of the BB-CG amplifiers, BB_1 through BB_8, are then ap-

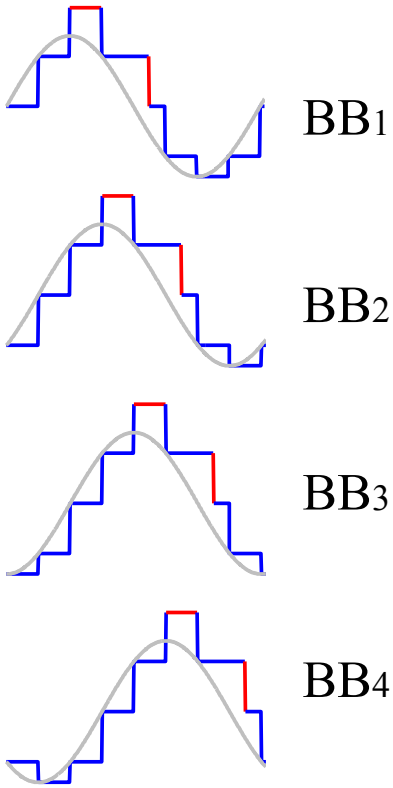


Figure 4.5: Relative 45° phase relationship between BB_1-BB_8 in the presence of gain and phase non-idealities. (BB_1-BB_4 are shown as illustrative example.)

plied to the baseband PMOS transconductors, which are configured as CS stages with gain ratios of 2 : 5 : 5 : 2. These stages are used to provide a 2^{nd}-stage of harmonic rejection.

BB_1-BB_8 are applied to baseband transconductors in the two 5-cells such that the phase shift between their outputs is 90° in order to obtain I/Q outputs (Fig. 4.4). The PMOS transconductors in the 7-cell are used for biasing only. The downconverted baseband signal with two-stage harmonic rejection is observed at the drains of the PMOS devices in the two 5-cells. The coupling capacitor C_C that couples the RF current to the switches, also ensures that the baseband signal does not re-enter the switch bank.

The net conversion gain from the RF inputs to the baseband outputs is the product of the conversion gain from the input of the RF transconductor to the output load of the BB-CG amplifiers, and the baseband gain from the outputs of the BB-CG amplifier to the drains of the harmonic-rejecting 2^{nd}-stage PMOS CS stages.

4.3 Circuit Implementation

4.3.1 The RF Transconductors

The input signal at RF is applied to three common-gate RF transconductors with gain coefficients in the ratio of 5 : 7 : 5. The 5-cell is shown in Fig. 4.6 while the 7-cell is shown in Fig. 4.7. An off-chip balun with a 1 : 1 impedance ratio is employed to convert a single-ended RF input to differential signals RF+ and RF-, which are shared by all three transconductor cells.

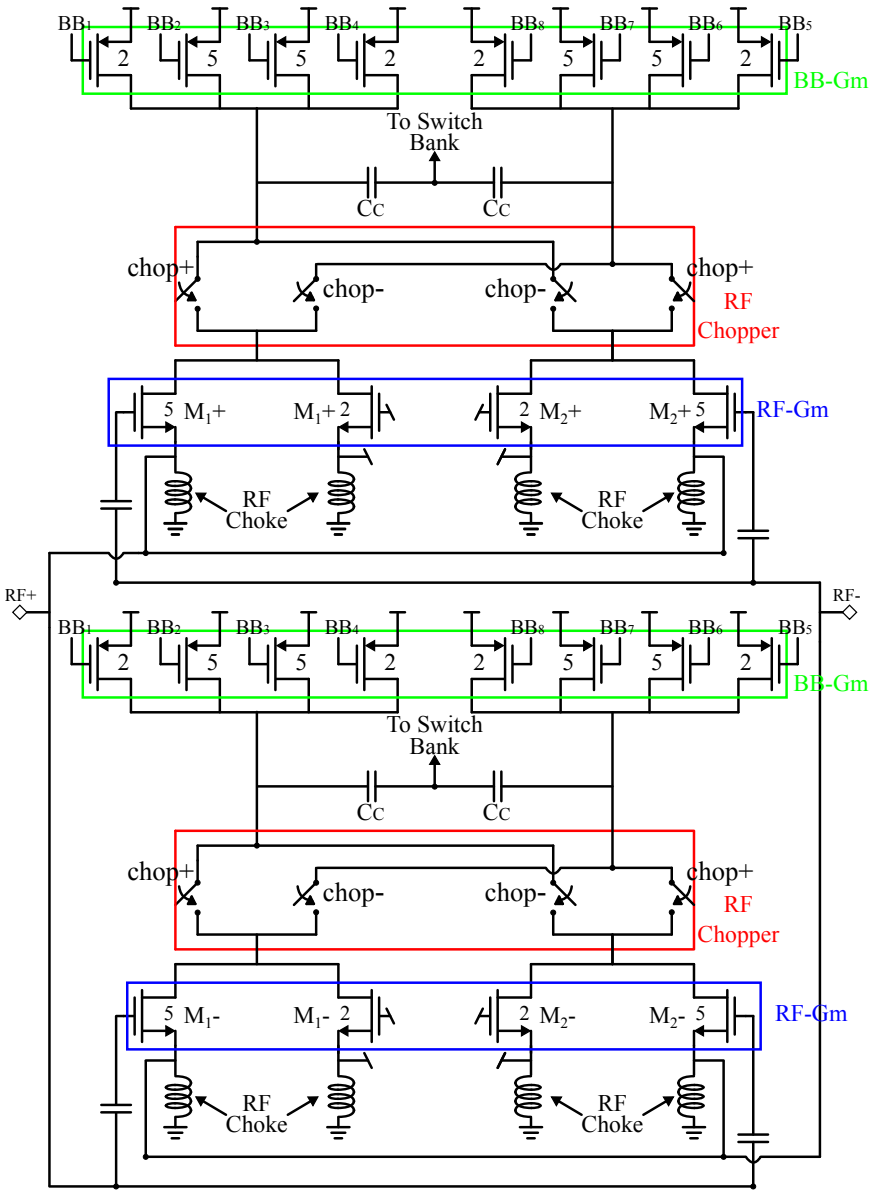


Figure 4.6: The 5-cell

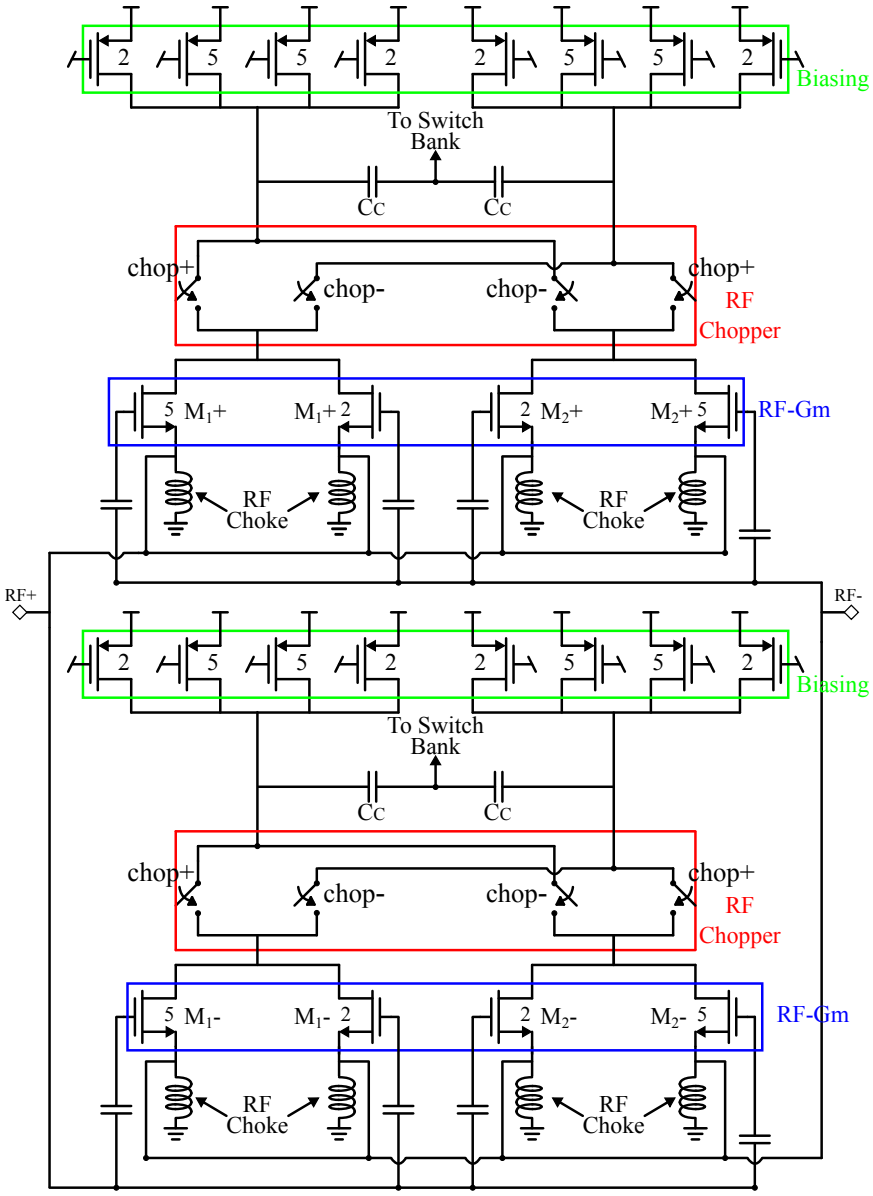


Figure 4.7: The 7-cell

Each transconductor consists of four NMOS devices, split into two pseudo-differential pairs. These devices are termed M_1+, M_2+, M_1- and M_2-. As can be observed from Fig. 4.6 and Fig. 4.7, the RF currents are in the same phase in the devices M_1+ and M_2+, and similarly in M_1- and M_2-. The RF current from these device pairs is coupled into the switch bank through capacitors C_C. Each of the differential RF inputs is coupled to the sources of two NMOS devices, and capacitively coupled to the gates of the other two devices. For example, RF+ is assumed to be coupled to the sources of M_1+, M_2+ and gates of M_1- and M_2-. The connections for RF- are similarly differentially cross-coupled. The cross-coupling doubles the effective gate-to-source voltage applied to each device, compared to applying the RF exclusively to the source or the gate nodes. Thus if each of the devices has a transconductance of g_m, the net differential input resistance contributed by the devices within any one G_M cell is $1/2g_m$. Since the three input transistors are in parallel, the effective input resistance seen by the balun is $1/2g_m^5 \parallel 1/2g_m^7 \parallel 1/2g_m^5$, where g_m^5 and g_m^7 are the transconductance of the 5-cell and 7-cell, respectively.

This resistance is made nominally equal to $50\,\Omega$ in the design. The baseband outputs are observed across the drains of the NMOS device pairs that are in-phase within the two 5-cells (Fig. 4.4). As can be observed from Fig. 4.6, the differential baseband signals across the drains of M_1+ and M_2+, and the drains of M_1- and M_2-, are canceled at the outputs of the coupling capacitors. This configuration is similar to that used in [41] and prevents the recirculation of the baseband signal in the mixer, which could otherwise be

upconverted and interfere with the RF inputs. As shown below, this configuration is also essential for ensuring harmonic rejection performance, and suppression of flicker noise. Note that in the 5-cell, the devices that provide transconductance are of size 5X. Two additional devices of size 2X are employed in parallel to the devices of size 5X. This ensures that the effective output resistance looking into the NMOS devices is nearly identical in the 7-cell and 5-cells, which is important for ensuring harmonic rejection provided by the first stage, and minimizing mismatch for common-mode biasing.

4.3.1.1 Flicker Noise Suppression

It is desirable to use minimum channel-length devices to implement the RF transconductors, for enhancing the frequency response. However this choice makes low frequency flicker-noise a critical consideration in the proposed bias-shared 2-stage HRM. This is the case since the input NMOS transconductors are directly coupled to the PMOS devices, and cannot utilize ac-coupling between RF and baseband stages to mitigate their low-frequency noise.

In order to mitigate the impact of NMOS flicker noise, a current-commutating chopper is employed. The drains of two RF (NMOS) transistors with the same phase are connected to a double-balanced mixer indicated as the "RF Chopper"' in Fig. 4.6. The devices within the chopper are either ON, in the linear region, or OFF, in response to an externally applied LO waveform. The chopper outputs are tied to the outputs of the baseband stage in Fig. 4.6. The NMOS devices connected to a particular chopper conduct

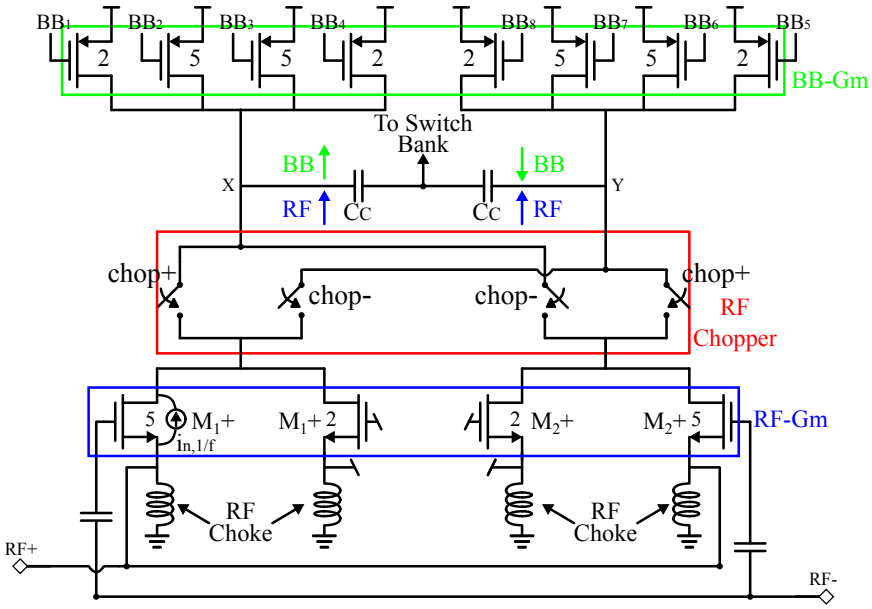


Figure 4.8: The proposed Gm-cell employing phase domain orthogonality and chopping

RF current in the same phase. Therefore, the chopper has no impact on the RF current itself.

Consider the flicker-noise current from the NMOS devices with size 5X in Fig. 4.8, which we term $i_{n,1/f}$. This noise current is coupled to nodes X and Y as follows:

$$i^X_{n,1/f} = i_{n,1/f} \times chop^+(t) \tag{4.7}$$

$$i^Y_{n,1/f} = i_{n,1/f} \times chop^-(t) \tag{4.8}$$

Since the final baseband outputs is observed differentially across nodes X and Y, it is equivalent that $i_{n,1/f}$ being multiplied by $chop(t) = chop^+(t) - chop^-(t)$ (Fig. 4.9). The RF chopper thus frequency translates $i_{n,1/f}$ to the chopping

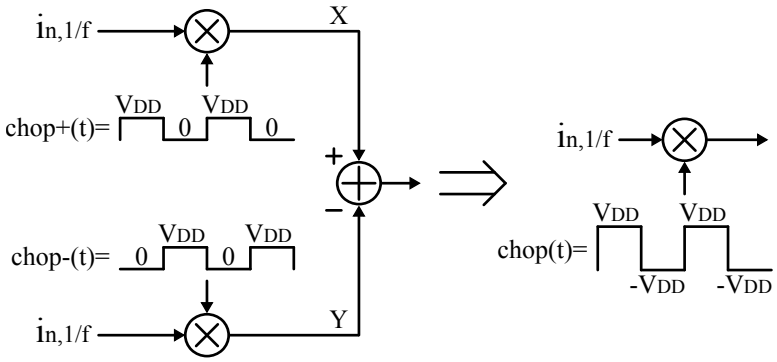


Figure 4.9: Effect of RF chopper on flicker noise

frequency f_{chop} and its odd harmonics, since $chop(t)$ does not contain any even harmonics. As a result, the flicker noise $i_{n,1/f}$ will not appear at baseband. Through proper choice of f_{chop}, it can also be isolated from the RF signal. The chopper devices introduce small additional parasitic capacitance, however the RF current flows into a low-impedance node of the BB-CG stage and hence the extra parasitic does not have a significant impact on the RF response.

4.3.1.2 Common-Mode Biasing

The common-mode voltage is compared to an external reference V_{REF} in the 7-cell, using a differential amplifier (Fig. 4.10). The output of the differential amplifier, V_{CMFB}, is fed back to the CG stage, and is used to control the common-mode setting in all three RF transconductors. Only the common-mode of the 7-cell is sensed, while the common-mode in the 5-cells is set by replica biasing. The use of the two extra devices per 5-cell ensures that for DC, all transconductor cells are identical, which is essential for employing replica bias. The common-mode voltages of these cells are detected externally

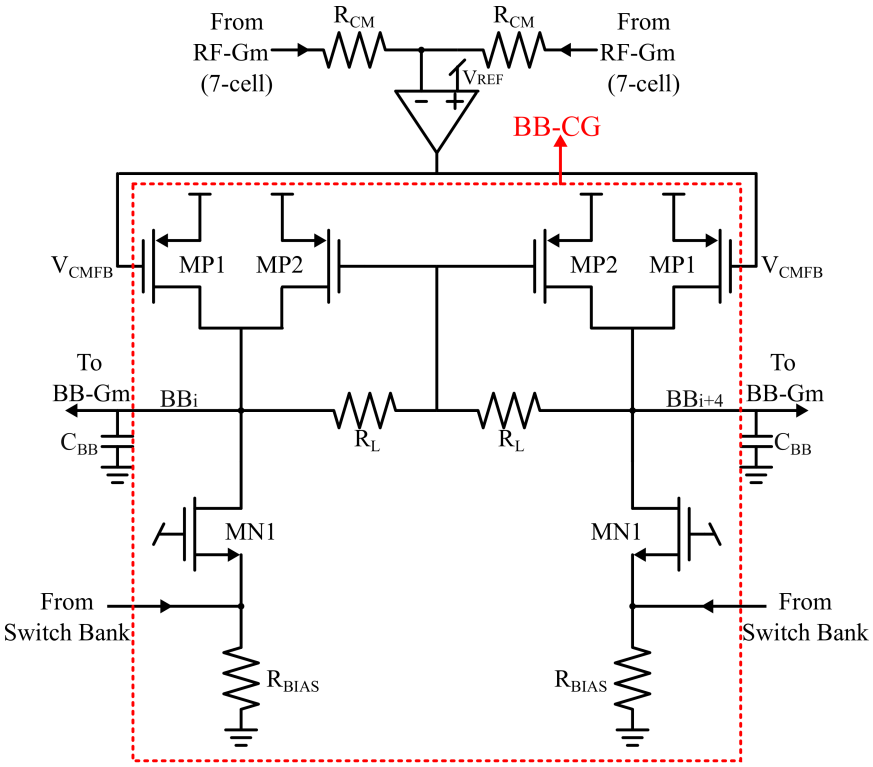


Figure 4.10: Common-mode biasing

on the board, at the drains of the two 5-cells, which can also be used for fine common-mode voltage control.

4.3.2 The Baseband Stage

In the 7-cell, PMOS devices are used only to supply the DC bias current to the RF transconductors. In the 5-cells, the PMOS devices used to bias the RF transconductors are also configured as baseband common-source amplifiers that provide a 2^{nd}-stage of harmonic rejection (Fig. 4.6). The PMOS transistors are configured with width ratios of 2:5:5:2, and combine four differential

phases from the CG buffer outputs BB1:4. The PMOS transistors that bias one of the 5-cells are used to provide the I-path outputs, while those biasing the other provide the Q-path outputs (Fig. 4.4). This is achieved through application of appropriate phases of the CG outputs to the PMOS devices.

An additional advantage that arises from the use of $2:5:5:2$ topology in the I and Q paths is that the total capacitance seen by the CG-stage loads is identical on all loads. The CG loads connected to size 2 devices in the I-side are connected to size 5 devices on the Q-side and vice versa. This would not be the case if cells with the ratio $2:3:2$ or $5:7:5$ had been used in the baseband stage for both I and Q sides. This aspect of the design is critical to maximizing the HRR.

The PMOS current source used to bias the 7-cell has a size of 14X. The use of the additional 2X sized devices in the 5-cells, ensures that the ratio of the PMOS device area to the NMOS device area is identical in the two types of RF transconductor cells.

The baseband signal is prevented from re-entering the switch bank by using the above arrangement of common-mode RF transconductor pairs along with differential PMOS devices, as noted above. Additionally, ac-coupling between the baseband devices and the switch bank also helps to mitigate the recirculation of baseband signals.

4.3.3 Switch Bank with Re-timing

Switch banks with re-timing (Fig. 2.8) are used in this design. This desensitizes the mismatch amongst the gain-steering switches. The mismatch among the re-timing switches is further suppressed by the 2^{nd}-stage harmonic rejection, as discussed in Sec. 4.2.2.

4.3.4 The Common-Gate (CG) Stages

The outputs of the switch banks are applied to CG amplifiers (Fig. 4.4), that are designed to provide an input impedance that is low relative to the output resistance of the RF transconductors. This reduces sensitivity to parasitic capacitance at the drain nodes of the RF transconductors, thereby enhancing the operating bandwidth.

The CG stages are implemented using NMOS transistors. The gates of these devices are biased externally (Fig. 4.10). The bias current is determined by this external bias voltage and the resistor R_{BIAS}. A resistor is used for setting the bias current instead of an active current source, to minimize flicker noise.

The CG NMOS devices are arranged in pseudo-differential pairs, and are driven by differential outputs from the switch bank. The drains of these devices are biased using PMOS loads which consist of two pairs of transistors. One pair, consisting of transistors MP2, provides low-impedance for common-mode signals while it presents a high impedance for differential signals. A chopper may also be included to avoid potential degradation of low-frequency

noise performance, that can result from amplification of the flicker noise of the PMOS load devices at the baseband outputs due to this current scaling.

The second pair of transistors MP1 in the PMOS load is driven by the common-mode feedback amplifier (Sec. 4.3.1.2). The voltage V_{CMFB} regulates the DC through these devices, and hence controls the gate-to-source voltage of MP1 and MP2. This gate-to-source voltage sets the DC of the PMOS current sources in the 7-cell in the RF stage (Fig. 4.7). In this way a negative feedback loop is set up for ensuring that the common-mode voltage at the drains of the RF transconductors equals V_{REF}. Since the total PMOS and NMOS device sizes are identical in the cells shown in Fig. 4.6 and Fig. 4.7, the voltage bias at the PMOS drain nodes of 5-cells in Fig. 4.6 can be set by replica-biasing (Sec. 4.3.1.2).

4.4 Performance of the Bias-Shared 2-Stage HRM

Harmonic-rejection in the two-stage approach with re-timing was briefly discussed in Sec. 4.2. In this section we will focus on additional issues relating to harmonic rejection, including those that arise due to the use of bias-sharing.

4.4.1 Second Harmonic Rejection

While bias-sharing significantly reduces power dissipation, it also introduces new design considerations. There is potential for the down-converted currents to re-enter the passive mixer stage at nodes BB-I and BB-Q in Fig. 4.4. Such a recirculation could lead to an upconversion of the down-converted

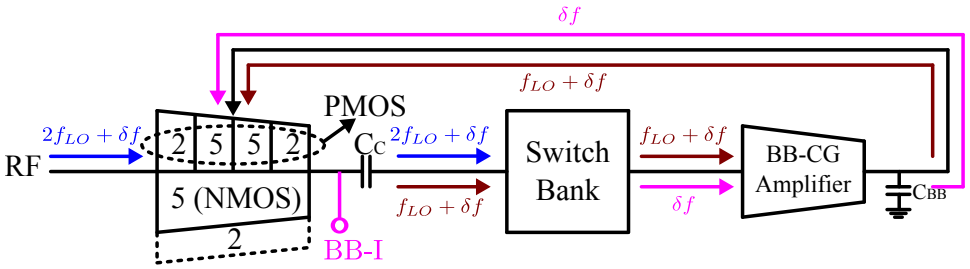


Figure 4.11: Potential for downconversion of interference at $2f_{LO}$ to f_{LO}, and to baseband

baseband signal, which could then lead to self-interference. The coupling capacitor C_C helps to mitigate this effect.

By a similar process, RF interferers around $2f_{LO}$ could experience two downconversions to baseband, thereby leading to non-ideal 2^{nd}-order harmonic-rejection (HR), even though a fully-differential design is employed. Consider an input at frequency $2f_{LO}+\delta f$ applied to the RF inputs in Fig. 4.11. Assuming perfect differential balance, there is ideally no second harmonic in the downconversion LO. Further assuming perfect rejection of $3f_{LO}$ and $5f_{LO}$, the input is downconverted by f_{LO} to a frequency of $f_{LO}+\delta f$. This downconverted signal now appears at the inputs to the switch bank, where it can be downconverted to baseband and appear at frequency of δf (Fig. 4.11). This would lead to non-ideal downconversion by the second harmonic of f_{LO}, i.e. $2f_{LO}$.

The Gm cell shown in Fig. 4.6 effectively addresses this issue. As illustrated in Fig. 4.12, differential baseband PMOS devices are used as loads for NMOS RF devices that are in-phase. Thus the downconverted signal at

$f_{LO} + \delta f$ at the outputs of the PMOS devices, appears as a differential-mode signal, and hence gets canceled to a level set by component matching at the input nodes of the switch bank. This is the case since the inputs to the switch bank, after C_C, appear as an ac-ground to any differential signals at the PMOS outputs. This component can be further suppressed by the filtering provided by the capacitor C_{BB} at the load of the BB-CG stage (Fig. 4.11).

This phase-domain orthogonality also prevents the desired baseband signals from re-entering the switch banks. It is noted that the required transconductance at RF is simply split into two-halves in this configuration. Therefore the two NMOS RF transistors each have half the area and bias current of the required RF transconductor device. As such, this configuration does not increase power dissipation or area. This phase-domain orthogonality, namely the use of common-mode RF signals and differential baseband signals, is similar to that used in [41] and [42].

4.4.2 Relative Output Resistance of the 5-Cell and 7-Cell

Output resistance of transconductors is a consideration in general implementations of 2-stage HRMs, including those not employing bias-reuse. Consider the outputs of the 5-cell and 7-cell. The NMOS transistors in these cells employ minimum channel length, and therefore primarily determine the effective resistance looking back into these nodes. Assume that the resistance looking back into the RF transconductors is given by R_{RF}^5 and R_{RF}^7, depending on whether a switch looks back into the 5-cell or the 7-cell. The switches

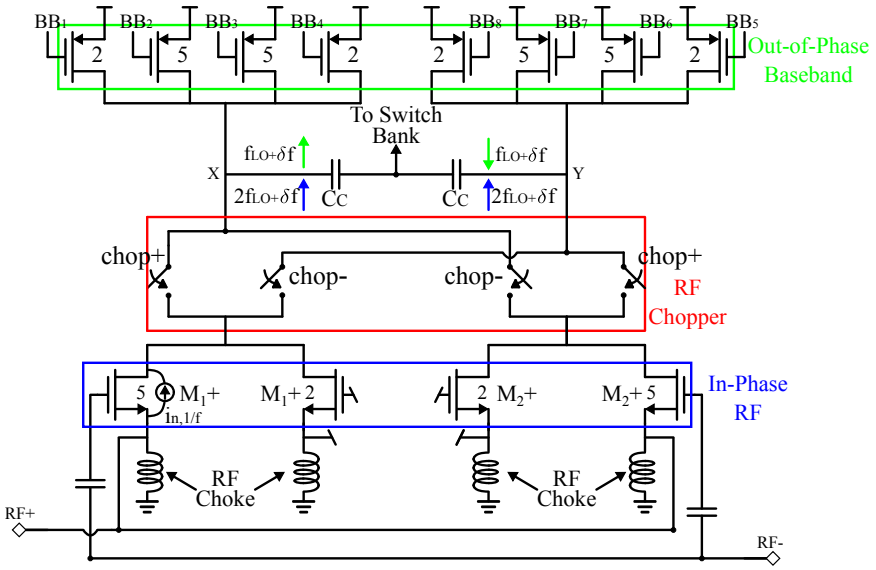


Figure 4.12: Improvement of 2^{nd} harmonic rejection through phase-domain orthogonality

that have a zero input in the 0:5:7:5 input stage see an infinitely large effective resistance, since they are not connected to a transconductor, although in a more precise design, a dummy NMOS transconductor without any signal may also be employed. The switch bank is terminated into a resistive load R_{BB}, that includes the small-signal resistance looking into the BB-CG source nodes, and the switch ON resistance.

The drain nodes of the 5-cell sees an effective resistance of $R_{RF}^5 \parallel R_{BB}$, while those of 7-cell sees $R_{RF}^7 \parallel R_{BB}$. The design is supposed to apply a gain sequence of 0:5:7:5:0:-5:-7:-5 to the RF current downconverted to any one baseband node, which approximates the ratio $1 : \sqrt{2} : 1$ by $1 : 1.4 : 1$. In reality, the signal experiences gain magnitude ratios of $5R_{RF}^5/(R_{BB} + R_{RF}^5)$

and $7R_{RF}^7/(R_{BB}+R_{RF}^7)$ from the 5-cell and 7-cell respectively. The effective gain magnitude ratio is thus

$$1 : 1.4 \times \frac{R_{RF}^7(R_{BB}+R_{RF}^5)}{R_{RF}^5(R_{BB}+R_{RF}^7)} : 1.$$

If $R_{BB} \ll R_{RF}^5$ and $R_{BB} \ll R_{RF}^7$, the gain sequence is almost ideally 0:5:7:5:0:-5:-7:-5. On the other hand, if this is not the case, the gain ratios will be different from this design choice.

Consider the case where the width ratio of the NMOS devices in the 5-cell and 7-cell is $5 : 7$. For this choice, $R_{RF}^7 = (5/7)R_{RF}^5$, and the gain magnitude ratio is modified to $1 : 1.4 - \delta : 1$, where δ is a small positive error term. This degrades the HRR compared to the design choice of $1 : 1.4 : 1$. Interestingly a design choice of $2 : 3 : 2$, which yields a normalized ratio of $1 : 1.5 : 1$ is actually helped by the difference in output resistance r_o, if the devices are sized in the ratio of $2 : 3$. However, variation in device r_o will introduce uncertainty in the HRR.

The device size of the RF transconductors in this design is kept identical. In the 5-cell (Fig. 4.6), NMOS devices of size 2X are used in shunt with the 5X devices that operate as transconductors, in order to provide a total device size of 7X, looking back into the transconductor from the switching devices. The effective output resistance of the 5-cell and 7-cell is thus made nearly identical. A difference remains in the output resistance, since cross-coupling cannot be utilized in the 2X devices for the 5-cell. The error caused by this is small and is traded-off against the ability to keep the layouts of the

three transconductors identical.

4.4.3 Noise and Linearity Performance

The noise and linearity performance of the receiver is similar to that achieved from cascading an RF and baseband amplifier, with an HRM-based downconverter. The flicker noise of the RF transistors is mitigated as described in Sec. 4.3.1.1. The high-frequency noise in these cells at RF enters the switch bank through C_C, where it is downconverted to baseband, and appears at the output through the baseband PMOS transconductors. The baseband noise of the PMOS transconductors and the BB-CG devices similarly appears at the outputs.

The use of harmonic rejection in the 1^{st}-stage introduces a noise figure penalty. Consider the use of three transconductors, two 5-cells and one 7-cell, that are connected in shunt and provide in-phase output currents. The devices are sized in the ratio $5:7:5$. If the signal current in a unit sized device is i_{rf}, then the total current at the output of these devices would be $17i_{rf}$. If the noise current of a unit sized device is $\overline{i_n^2}$ A^2/Hz, the total SNR at the output is $17\left(i_{rf}^2/\overline{i_n^2}\right)$.

If we now assume that the signal currents provided by the 5-cells experience phase offsets of $\pm 45^o$ relative to that of the 7-cell from the effective LO waveforms applied to them, then the IF output current phasors from the 1^{st}-stage for the three cells, are scaled by $5e^{-j45^o}$, $7e^{j0^o}$ and $5e^{j45^o}$. Combination of these phasors provides a net output current of magnitude $(7+5\sqrt{2})e^{j0^o}$, while

the imaginary components of the current phasors from the 5-cells mutually cancel. This cancellation is observed only in the signal path, and is not applicable to transconductor noise. The total output noise current thus stays identical to the above case, thus yielding an effective SNR of $\left\{(7+5\sqrt{2})^2/17\right\}(i_{rf}^2/\overline{i_n^2})$, or $11.64(i_{rf}^2/\overline{i_n^2})$. In our design we add dummy devices to equalize the output resistance of the G_M cells. This further decreases the output SNR to $\left\{(7+5\sqrt{2})^2/21\right\}(i_{rf}^2/\overline{i_n^2})$, or $9.4(i_{rf}^2/\overline{i_n^2})$. This represents a degradation of 2.56 dB in the SNR compared to the case where all transconductors conduct in-phase. This cost would not be incurred in a single-stage HRM design. On the other hand, in a single-stage HRM, harmonics are not rejected at the input to the baseband, and as such can impose a linearity penalty. This is fundamentally a trade-off between harmonic rejection performance and noise figure. It is also important to note that harmonic rejection in the 1^{st}-stage does not reject the noise around the LO harmonics arising from the three transconductors, at baseband.

Linearity of the design is equivalent to that of a broadband RF stage cascaded with a baseband stage with an inter-stage 1^{st}-order LPF. The RF load is relatively small, since the switch bank is terminated in BB-CG stages. This ensures that the RF voltage at the NMOS drains is small. On the other hand, the baseband PMOS devices operate as voltage amplifiers. Primary compression point limitation appears from voltage compression at baseband at the output nodes (NMOS/PMOS drains in Fig. 4.6). The out-of-band linearity is assisted by the 1^{st}-order pole provided by the capacitor C_{BB} in

Fig. 4.4.

4.5 Experimental Results

The bias-sharing HRM is implemented in a 130nm CMOS process. The master clock is derived from an externally applied sinusoidal signal, and has a frequency $f_{CLK} = 8f_{LO}$. An off-chip balun converts this to differential clocks and an on-chip clock buffer is used to generate 50% duty-cycle square waves, which are then used as the clocks for switch banks. The RF chopper also uses a chopping frequency of $f_{chop} = 8f_{LO}$.

The active chip area was approximately 500x700 μm^2 (Fig. 4.13). The design was measured in a TQFP package on a PCB. The chip provided base-band differential I-Q outputs, which were converted to a single-ended output using an external differential-to-single-ended unity gain buffer.

A conversion gain of 35.8 dB at f_{LO} of 100 MHz is measured with approximately $\pm$0.5 dB mismatch between the I and Q sides. For an f_{LO} of 250 MHz, the gain is approximately 32 dB (Fig. 4.14). This gain decrease is because of a switched-capacitor ($\propto 1/f_s C_{par}$) resistor that appears due to chopping across the loads of the PMOS devices. The noise figure was approximately 11.5 dB (Fig. 4.15), and the flicker noise corner frequency with RF choppers enabled was observed to be nearly 82 kHz. Turning off the RF chopper yielded a flicker noise corner of 240 kHz. The S_{11} is measured to be better than -10 dB up to 800 MHz.

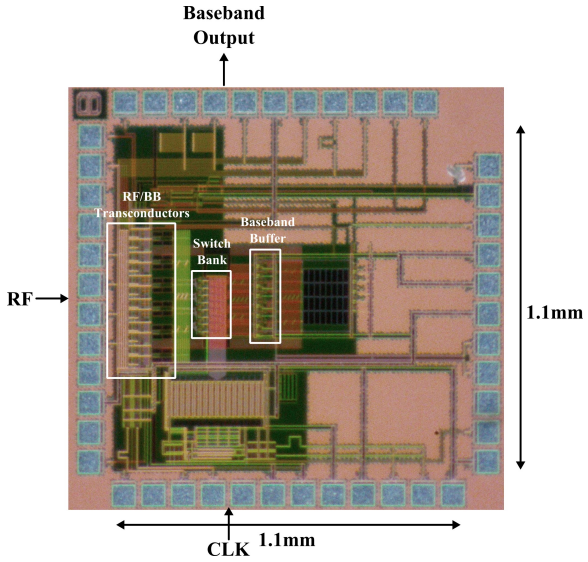


Figure 4.13: Die photograph

HRR was measured over 8 parts, and found to be consistently better than 60 dB, for harmonics $2f_{LO}$ to $6f_{LO}$. The measurement result is shown in Fig. 4.16 for f_{LO}=100 MHz and f_{LO}=250 MHz, respectively. This performance is achieved without any calibration, and shows low sensitivity to the biasing state of the HRM. Filtering provided by C_{BB} enhances rejection around $2f_{LO}$, but is not required for other harmonics.

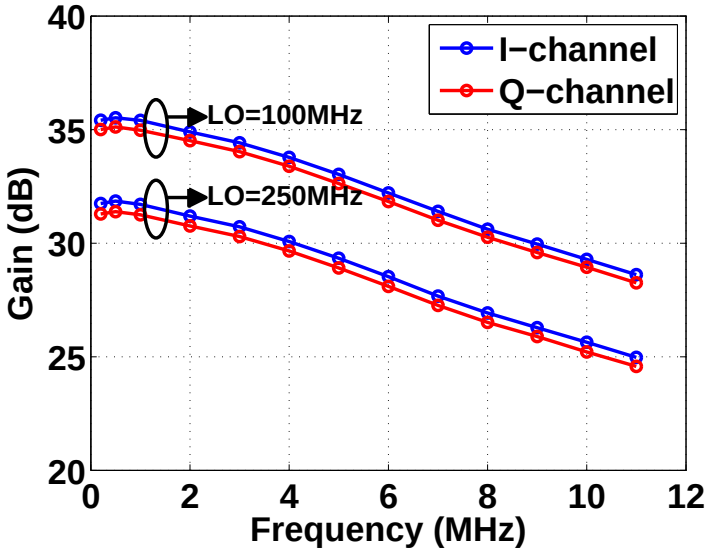


Figure 4.14: Measured conversion gain for f_{LO}=100 MHz and f_{LO}=250 MHz

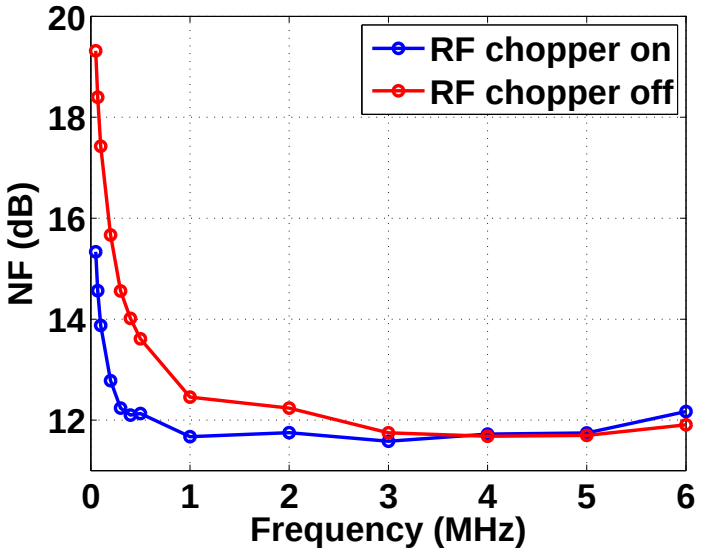
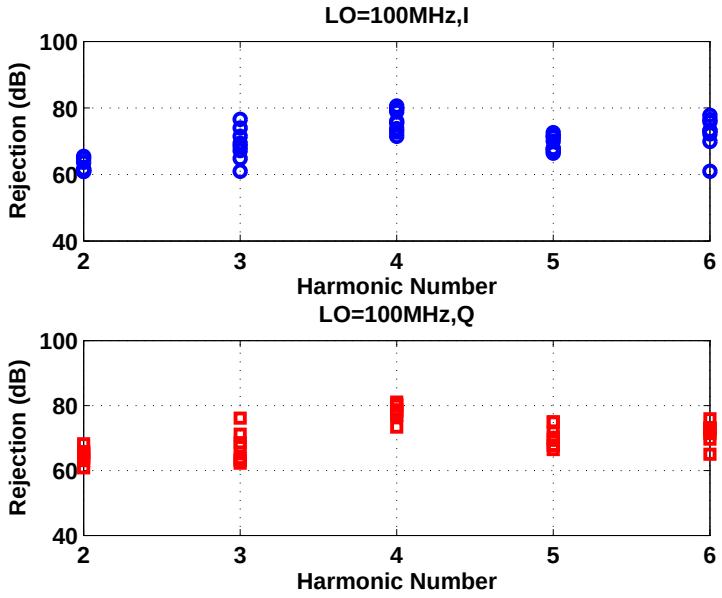
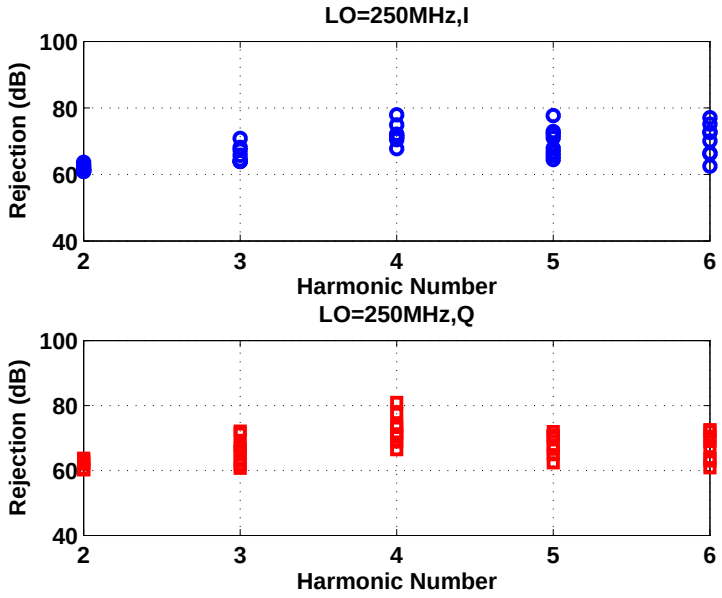


Figure 4.15: Measured NF with and without RF chopper



(a)



(b)

Figure 4.16: Measurement of HRR for (a) LO=100 MHz (b) LO=250 MHz

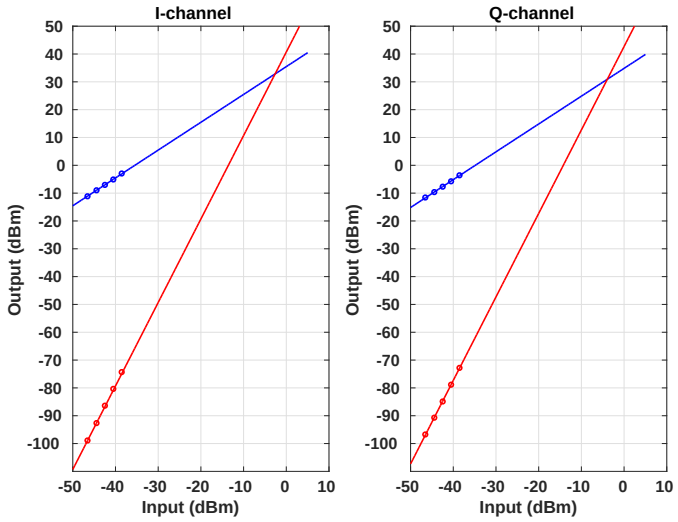


Figure 4.17: Measured out-of-band IIP3

Out-of-band IIP3 is measured to be approximately -3 dBm (Fig. 4.17). It can be further improved by using capacitive loading at the BB-CG source nodes to provide additional filtering. This capacitor was not included in the design. By including this, an OOB-IIP3 enhancement of 12 dB, from -4 dBm to 8 dBm, was observed in simulation. The IIP2 is measured to be around +49 dBm (Fig. 4.18) and the output compression is around -4 dBV (Fig. 4.19).

The power dissipation in the RF stage was 11.7 mW, and 2.7 mW in the baseband CG stages. The power in the clock generator was 9.7 mW for f_{CLK} of 800 MHz. The RF chopper consumes around 6 mW and can be reduced by using a smaller driving buffer. Clock and RF chopper power are seen to scale linearly with f_{CLK}. Use of a faster technology, such as 65 nm CMOS, is expected to significantly reduce power dissipation, especially in the clock

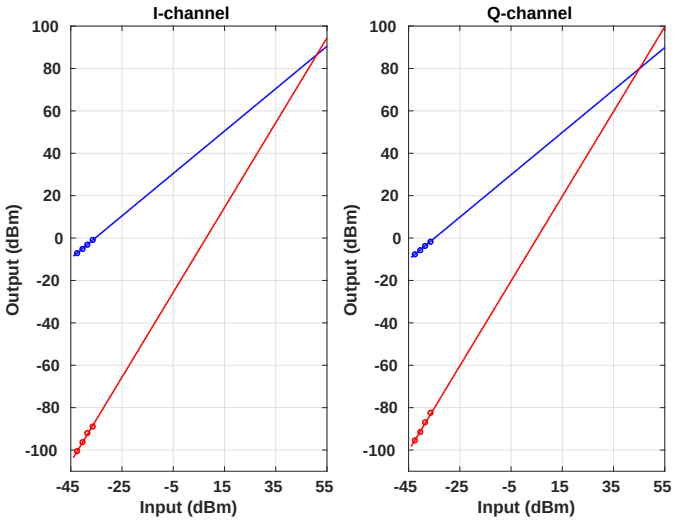


Figure 4.18: Measured out-of-band IIP2

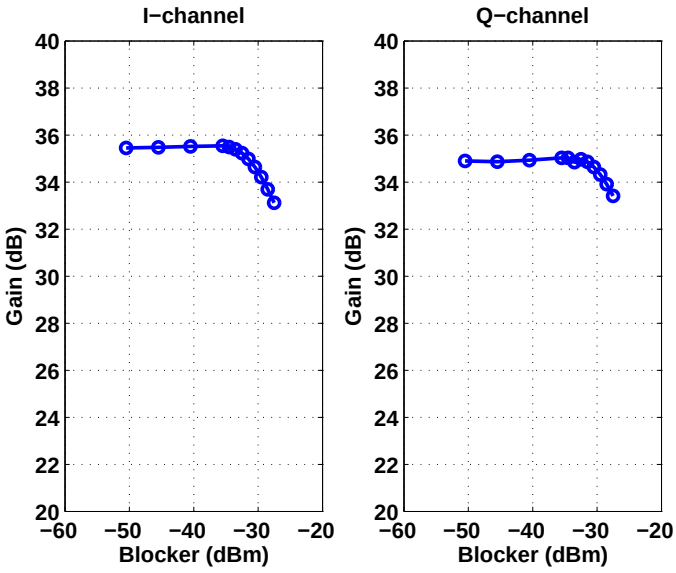


Figure 4.19: Measured in-band 1-dB compression

Table 4.1: Performance comparison

	This work	[10]	[43]	[44]
f_{LO} (MHz)	**100-250**	100-300	50-350	48-1000
Gain (dB)	**35.8-32**	19	3	15
DSB NF (dB)	**11.5**	11	13.5	12
OIP3 (dBV)	**22.8**†	21	6	23
HRR3 (dB)	>**61**	52	52	>60
HRR5 (dB)	>**62**	54	-	>60
Power (mW)	**14.4(A)** **15.7(D)**	91.8(A) 10.4(D)	34.8	93
Supply A/D (V)	**1.2/1.2**	2.7/1.3	1.2	1.5
Technology	**130nm**	110nm	90nm	130nm

†: Without load capacitor at CG input

generator and the RF chopper. A comparison to other recently published HR-based receivers and mixers in similar technology nodes is shown in Table 4.1.

4.6 Conclusion

A low-power HRM is demonstrated in this work. The approach shows the feasibility for using bias-sharing in HRMs, while achieving two-stage harmonic rejection. Mechanisms for potential performance degradation are identified, and design solutions are demonstrated.

Chapter 5

Conclusion

5.1 Review

Broadband channelizers divide the input spectrum into multiple sub-bands, such that the sub-bands can be digitized by ADCs that operate at a lower sampling rate. In this dissertation, circuit techniques that can be employed in the implementation of broadband channelizers were described. The proposed interference cancellation technique helps to relax the dynamic range requirement of the channelizer front-end. The proposed bias-shared HRM reduces the power consumption of the down-conversion mixers that are used in the channelizer. These techniques can also be applied to flexible receivers, such as software-defined radios.

In Chapter 2, a feedback-based interference canceler is proposed. A frequency-translation loop selects the interferer and subtracts it from the input. Through the use of frequency synthesis capable harmonic rejection mixers, in both the down-conversion and up-conversion paths, the harmonic response and required synthesizer tuning range of the design are reduced compared to conventional switch-based N-path filters. The implementation of the feedback-based interference canceler with 8-phase AFS-HRMs was described.

In Chapter 3, a harmonic-transfer-matrix based approach was used to analyze the performance of a 4-path band-pass filter and the proposed interference canceler. A harmonic transfer matrix is a frequency domain technique that can be used in the analysis of linear periodic time-varying systems. It is also shown in the appendices that the resulting algebraic equations can be solved compactly by means of signal flow graphs and Mason's gain formula. Compared to the state-space method, the approach can provide greater design insights to circuit designers. For example, the analysis clearly shows that the maximum achievable rejection of the proposed interference canceler can be improved if out-of-band harmonics are suppressed, which is difficult to derive by using the state-space method.

In Chapter 4, a bias-shared HRM is proposed that reduces the power consumption by sharing the bias current between the RF and baseband transconductors in a 2-stage HRM. The 2-stage architecture desensitizes the impact of gain non-idealities on the HRR, while the clock re-timing technique mitigates the effect of phase mismatch on the HRR. Phase-domain orthogonality is proposed to ensure good even-order HRR and chopping is used to mitigate the potential flicker noise performance degradation due to bias-sharing. The proposed bias-shared HRM was shown to achieve state-of-the-art harmonic rejection without calibration or harmonic filtering, while consuming significantly lower power.

5.2 Future Work

The proposed interference canceler equivalently gives a second-order notch response around the LO frequency by using a first-order RC low-pass filter at baseband. Higher-order low-pass filters can be used in the baseband that can give sharper notch response. However, the phase margin of such a feedback system is a concern in order to ensure stability. One way to design such a feedback system is starting from the desired closed-loop response, and then deriving the corresponding baseband low-pass filter transfer function. Through the use of the HTM for deriving the closed-loop response, the baseband transfer function can be calculated analytically.

The proposed bias-shared HRM uses NMOS as RF transconductors and PMOS as baseband transconductors. The dynamic range per power can be further improved if both NMOS and PMOS can be used at RF and baseband. Furthermore, if the low-impedance baseband buffer can also be merged into these transconductors, a 2-stage HRM with excellent power efficiency can be achieved. Such a circuit can greatly save power dissipation, while avoiding calibration that is required in conventional HRMs.

Appendices

Appendix A

Derivation of the Harmonic Transfer Function for a 4-path Bandpass Filter

The derivation of Eq. (3.23) is described below.

Under the assumption that the BB-LPF has large attenuation for frequencies greater than f_{LO}, the HTM $\widetilde{H_{BB}}(s)$ contains only one non-zero term $H_0(s)$

$$\widetilde{H_{BB}}(s) = Z_C(s) = \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & \frac{1}{(s-j\omega_{LO})C} & 0 & 0 & \cdots \\ \cdots & 0 & \frac{1}{sC} & 0 & \cdots \\ \cdots & 0 & 0 & \frac{1}{(s+j\omega_{LO})C} & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix}$$

$$\approx \begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & 0 & 0 & 0 & \cdots \\ \cdots & 0 & \frac{1}{sC} & 0 & \cdots \\ \cdots & 0 & 0 & 0 & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix}. \tag{A.1}$$

The goal here is to express $i_{in}(s + j\omega_{LO})$, which is the frequency component around ω_{LO} for i_{in}, in terms of the frequency components around ω_{LO} for V_{in}, $V_{in}(s + j\omega_{LO})$, where V_{in} and i_{in} are denoted in Fig. 3.3. Assuming that the 4 paths are perfectly matched, the fundamental frequency of i_{in} will

be $4f_{LO}$ because of symmetry. Therefore, i_{in} can be represented as

$$i_{in} = \begin{bmatrix} \vdots \\ i_{in}(s - j3\omega_{LO}) \\ i_{in}(s + j\omega_{LO}) \\ i_{in}(s + j5\omega_{LO}) \\ \vdots \end{bmatrix}. \tag{A.2}$$

Using Eq (A.1) and (A.2), Eq (3.22) can be represented by the following signal flow graph

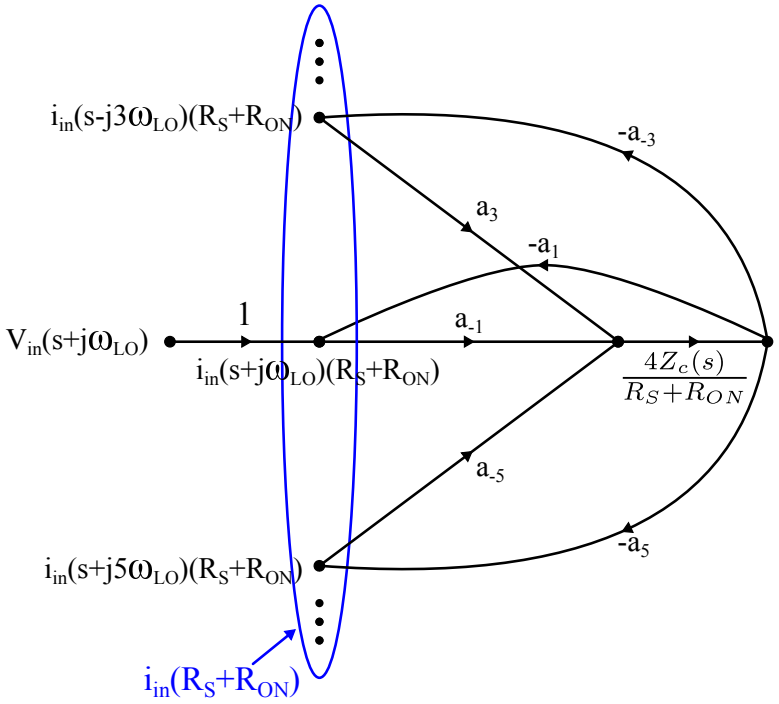


Figure A.1: Signal flow graph representation of the 4-path BPF

According to Mason's rule [45], the gain from an input node y_{in} to an

output node y_{out} can be written as

$$G = \frac{y_{out}}{y_{in}} = \frac{\sum_k G_k \Delta_k}{\Delta} \tag{A.3}$$

where

- Δ = determinant of the graph $= 1 - \Sigma L_i + \Sigma L_i L_j - \cdots$
  - L_i = loop gain of each closed loop in the graph
  - $L_i L_j$ = product of the loop gains of any two non-touching loops in the graph
- G_k = path gain of the k$^{\text{th}}$ forward path from y_{in} to y_{out}
- Δ_k = determinant of the graph after removing all nodes along the k$^{\text{th}}$ forward path

In Fig. A.1, it can be seen that there are no non-touching loops, hence we have

$$\begin{aligned} \Delta &= 1 + a_{-1}\frac{4Z_C(s)}{R_S + R_{ON}}a_1 + a_3\frac{4Z_C(s)}{R_S + R_{ON}}a_{-3} + a_{-5}\frac{4Z_C(s)}{R_S + R_{ON}}a_5 + \cdots \\ &= 1 + (|a_1|^2 + |a_3|^2 + |a_5|^2 + \cdots)\frac{4Z_C(s)}{R_S + R_{ON}}. \end{aligned} \tag{A.4}$$

There is only one forward path from $V_{in}(s + j\omega_{LO})$ to $i_{in}(s + j\omega_{LO})(R_S + R_{ON})$ with gain $G_1 = 1$. After removing all nodes along this path, the resulting

graph will have a determinant Δ_1

$$\begin{aligned}\Delta_1 &= 1 + a_3\frac{4Z_C(s)}{R_S+R_{ON}}a_{-3} + a_{-5}\frac{4Z_C(s)}{R_S+R_{ON}}a_5 + \cdots \\ &= 1 + (|a_3|^2 + |a_5|^2 + \cdots)\frac{4Z_C(s)}{R_S+R_{ON}} \end{aligned} \tag{A.5}$$

By using Eq (A.3) and substituting $Z_C(s)$ with $\dfrac{1}{sC}$, we have therefore

$$\begin{aligned} i_{in}(s+j\omega_{LO}) = &\frac{1 + (|a_3|^2 + |a_5|^2 + \cdots)\dfrac{4}{sC(R_S+R_{ON})}}{1 + (|a_1|^2 + |a_3|^2 + |a_5|^2 + \cdots)\dfrac{4}{sC(R_S+R_{ON})}} \\ &\times \frac{V_{in}(s+j\omega_{LO})}{R_S+R_{ON}}. \end{aligned} \tag{A.6}$$

which is the same as Eq (3.23).

Appendix B

Derivation of the Maximum Achievable Rejection of the Proposed Interference Canceler

The derivation of Eq. (3.33) is shown below. The corresponding signal flow graph is shown in Fig. B.1.

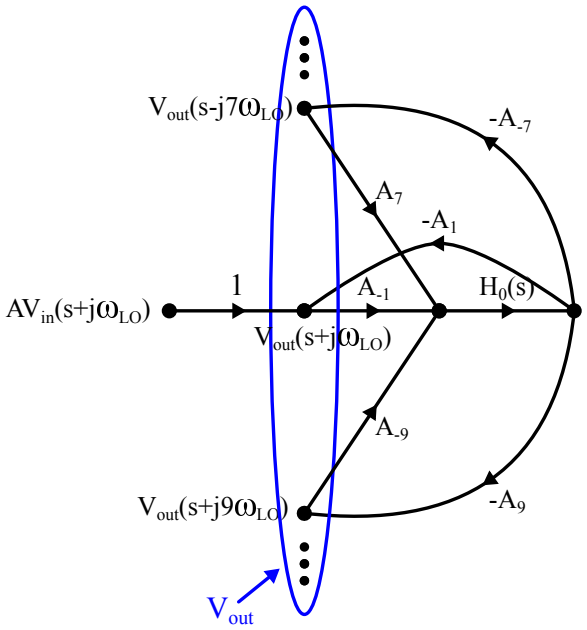


Figure B.1: Signal flow graph representation of the proposed interference canceler

Following a procedure similar to Appendix-A, we have

$$\begin{aligned}\Delta &= 1 + A_{-1}H_0(s)A_1 + A_7H_0(s)A_{-7} + A_{-9}H_0(s)A_9 + \cdots \\ &= 1 + H_0(s)(|A_1|^2 + |A_7|^2 + |A_9|^2 + \cdots). \end{aligned} \tag{B.1}$$

There is only one forward path from $AV_{in}(s + j\omega_{LO})$ to $V_{out}(s + j\omega_{LO})$ with gain $G_1 = 1$. After removing all nodes along this path, the resulting graph will have a determinant Δ_1

$$\begin{aligned}\Delta_1 &= 1 + A_7H_0(s)A_{-7} + A_{-9}H_0(s)A_9 + \cdots \\ &= 1 + H_0(s)(|A_7|^2 + |A_9|^2 + \cdots). \end{aligned} \tag{B.2}$$

By applying Mason's gain formula, we have therefore

$$\begin{aligned}V_{out}(s + j\omega_{LO}) = &\frac{1 + H_0(s)(|A_7|^2 + |A_9|^2 + ...)}{1 + H_0(s)(|A_1|^2 + |A_7|^2 + |A_9|^2 + ...)} \\ &\times AV_{in}(s + j\omega_{LO}). \end{aligned} \tag{B.3}$$

Bibliography

[1] J. Mitola, "The software radio architecture," *IEEE Communications Magazine*, vol. 33, no. 5, pp. 26–38, May 1995.

[2] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. A. Abidi, "An 800 MHz - 6 GHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec 2006.

[3] A. Abidi, "The path to the software-defined radio receiver," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.

[4] G. Ding, C. Dehollain, M. Declercq, and K. Azadet, "Frequency-interleaving technique for high-speed A/D conversion," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1, May 2003, pp. 857–860.

[5] S. Hoyos and B. Sadler, "Ultra-wideband analog-to-digital conversion via signal expansion," *IEEE Transactions on Vehicular Technology*, vol. 54, no. 5, pp. 1609–1622, Sept 2005.

[6] R. Gharpurey and P. Kinget, "Channelized front ends for broadband analog and RF signal processing with merged LO synthesis," in *Circuits and Systems Workshop,(DCAS), 2009 IEEE Dallas*, Oct 2009, pp. 1–4.

[7] V. Singh, T. Forbes, W. G. Ho, J. Ko, and R. Gharpurey, "A 16-band channelizer employing harmonic rejection mixers with enhanced image rejection," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sept 2014, pp. 1–4.

[8] J. A. Weldon, J. C. Rudell, L. Lin, R. S. Narayanaswami, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. R. Gray, "A 1.75 GHz highly-integrated narrow-band CMOS transmitter with harmonic-rejection mixers," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2001, pp. 160–161.

[9] Z. Ru, N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec 2009.

[10] A. A. Rafi and T. R. Viswanathan, "Harmonic rejection mixing techniques using clock-gating," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1862–1874, Aug 2013.

[11] T. Forbes, W. G. Ho, and R. Gharpurey, "Design and analysis of harmonic rejection mixers with programmable LO frequency," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2363–2374, Oct 2013.

[12] R. Gharpurey and S. Ayazian, "Feedforward interference cancellation in narrow-band receivers," in *2006 IEEE Dallas/CAS Workshop on Design, Applications, Integration and Software*, Oct 2006, pp. 67–70.

[13] S. Ayazian and R. Gharpurey, "Feedforward interference cancellation in radio receiver front-ends," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 902–906, Oct 2007.

[14] H. Darabi, "A blocker filtering technique for SAW-less wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2766–2773, Dec 2007.

[15] A. Safarian, A. Shameli, A. Rofougaran, M. Rofougaran, and F. de Flaviis, "Integrated blocker filtering RF front ends," in *IEEE RFIC Symp.*, June 2007, pp. 13–16.

[16] T. D. Werth, C. Schmits, and S. Heinen, "Active feedback interference cancellation in RF receiver front-ends," in *IEEE RFIC Symp.*, June 2009, pp. 379–382.

[17] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec 2006.

[18] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40nm CMOS highly linear 0.4-to-6GHz receiver resilient to 0dBm out-of-band blockers," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2011, pp. 62–64.

[19] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[20] A. Ghaffari, E. A. M. Klumperink, and B. Nauta, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, June 2013.

[21] A. Ghaffari, E. Klumperink, and B. Nauta, "8-path tunable RF notch filters for blocker suppression," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2012, pp. 76–78.

[22] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filter," *The Bell System Technical Journal*, vol. 39, no. 5, pp. 1321–1350, Sept 1960.

[23] A. Molnar, B. Lu, S. Lanzisera, B. W. Cook, and K. S. J. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *IEEE Custom Integrated Circuits Conference (CICC)*, Oct 2004, pp. 401–404.

[24] A. V. Oppenheim and R. W. Schafer, *Discrete-time signal processing*. Pearson Higher Education, 2010.

[25] T. Forbes and R. Gharpurey, "Embedded LO synthesis method in harmonic rejection mixers," in *IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2012, pp. 750–753.

[26] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Transactions on Audio and Electroacoustics*, vol. 19, no. 1, pp. 48–57, Mar 1971.

[27] W. G. Ho, V. Singh, T. Forbes, and R. Gharpurey, "An active interference canceler with reduced harmonic response and synthesizer tuning range," in *IEEE RFIC Symp.*, May 2015, pp. 383–386, © 2015 IEEE. Reprinted, with permission, from [W. G. Ho, V. Singh, T. Forbes and R. Gharpurey, An active interference canceler with reduced harmonic response and synthesizer tuning range, IEEE, RFIC symp., May 2015].

[28] A. A. Rafi, A. Piovaccari, P. Vancorenland, and T. Tuttle, "A harmonic rejection mixer robust to RF device mismatches," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2011, pp. 66–68.

[29] T. Hornak, K. Knudsen, A. Grzegorek, K. Nishimura, and W. McFarland, "An image-rejecting mixer and vector filter with 55-dB image rejection over process, temperature, and transistor mismatch," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp. 23–33, Jan 2001.

[30] R. Pullela, T. Sowlati, and D. Rozenblit, "Low flicker-noise quadrature mixer topology," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2006, pp. 1870–1879.

[31] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital integrated circuits*. Prentice hall Englewood Cliffs, 2002, vol. 2.

[32] M. Kaltiokallio, V. Saari, S. Kallioinen, A. Parssinen, and J. Ryynanen, "Wideband 2 to 6 GHz RF front-end with blocker filtering," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1636–1645, July 2012.

[33] A. V. Oppenheim, A. S. Willsky, and S. H. Nawab, *Signals and systems*. Pearson, 2014.

[34] L. A. Zadeh, "Time-varying networks, I," *Proceedings of the IRE*, vol. 49, no. 10, pp. 1488–1503, Oct 1961.

[35] P. Vanassche, G. Gielen, and W. Sansen, "Symbolic modeling of periodically time-varying systems using harmonic transfer matrices," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 9, pp. 1011–1024, Sep 2002.

[36] S. Hameed, M. Rachid, B. Daneshrad, and S. Pamarti, "Frequency-domain analysis of N -path filters using conversion matrices," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 1, pp. 74–78, Jan 2016.

[37] W.-G. Ho, T. Forbes, V. Singh, and R. Gharpurey, "An active interference cancellation technique with harmonic rejection for a broadband channelizer," in *IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2013.

[38] T. Forbes, "Circuit techniques for programmable broadband radio receivers," Ph.D. dissertation, University of Texas at Austin, December

2013.

[39] D. Ghosh and R. Gharpurey, "A power-efficient receiver architecture employing bias-current-shared RF and baseband with merged supply voltage domains and 1/f noise reduction," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 381–391, Feb 2012.

[40] W. G. Ho, T. Forbes, and R. Gharpurey, "A low-power two-stage harmonic rejection quadrature mixer employing bias-current reuse," in *IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2015, pp. 1–4, © 2015 IEEE. Reprinted, with permission, from [W. G. Ho, T. Forbes and R. Gharpurey, A low–power two–stage harmonic rejection quadrature mixer employing bias–current reuse, IEEE, MWSCAS symp., Aug 2015].

[41] J. Han and R. Gharpurey, "Recursive receiver down-converters with multiband feedback and gain-reuse," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1119–1131, May 2008.

[42] R. Srinivasan, W. G. Ho, T. Forbes, and R. Gharpurey, "A 2-stage recursive receiver optimized for low flicker noise corner," in *IEEE RFIC Symp.*, June 2014, pp. 47–50.

[43] C. Y. Cha, H. B. Lee, and K. K. O, "A TV-band harmonic rejection mixer adopting a g_m linearization technique," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 9, pp. 563–565, Sept 2009.

[44] I. Y. Lee, S. S. Lee, D. Im, S. Kim, J. Choi, S. G. Lee, and J. Ko, "A fully integrated TV tuner front-end with >3.1dB NF, >+31dBm OIP3, >83dB HRR3/5 and >68dB HRR7," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2014, pp. 70–71.

[45] S. J. Mason and Z. H. J, *Electronic Circuits, Signals, and Systems*. Wiley, 1960, vol. 1.

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